ATC260x Datasheet

Latest Version: 1.1

2012-06-10

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2. Contents

3. Revision History

Date	Revision	Description
2012-01-10	1.0	New Release
2012-06-10	1.1	Add ATC2603

4. Introduction

4.1 Overview

ATC260X is an integrated audio and power management subsystem IC family, which provides a cost effective, single-chip solution for portable multimedia systems. And ATC2605 with an Ethernet PHY build in.

The integrated audio CODEC provides all the necessary functions for high-quality recording and playback, stereo or multi-channel (including 5.1 or 7.1). Programmable on-chip amplifiers allow for the direct connection of headphones and microphones with a minimum of external components. A stereo Class D or Class AB dual mode amplifier is also build in. Digital microphone interface is supported.

ATC260X includes four programmable DC-DC converters, twelve low-dropout (LDO) regulators and two current limit switch to generate suitable supply voltages for each part of the system, on-chip PHY and audio CODEC as well as off-chip components such as a digital core, memory chips, WiFi and sensor modules. Each of these is voltage programmable. The ATC260X can be powered by a lithium battery, by a wall adaptor or USB.

An on-chip battery charger supports both trickle charging and fast (constant current, constant voltage) charging of single-cell Lithium batteries. The charge current, termination voltage, and charger time-out are programmable to suit different types of batteries.

Internal power management circuitry controls the start-up and shutdown sequencing of supply voltages, as well as sleep and wake-up. It also detects and handles conditions such as over-voltage, over-current.

The integrated Ethernet PHY is fully compliant with 100BASE-TX and 10BASE-T PMD level standards (IEEE 802.3u, FDDI-TP-PMD, and IEEE 802.3) , with RMII and SMII interface. This function is only included in ATC2605.

A 32.768kHz crystal oscillator should be supplied to ATC260X system to get an accuracy clock for real time clock (RTC) and an alarm function capable of waking up the system. The master clock can be input directly or generated by an crystal oscillator 24MHz or 25MHz.

Resistance Touch Panel, IR, multi-channel ADC capable of waking up function is also integrated.

All the information from the Master SOC is configured through SPI interface.

4.2 Feature

Audio CODEC

- 7.1 channel DAC, SNR (A-WEIGHTING)>98dB, THD<-80dB.
- Two stereo ADCs, SNR(A-WEIGHTING)>91dB, THD<-82dB, for Supporting multi channels DV microphone recording, difference or single-ended input both supported.
- Stereo 20mW PA (Power Amplifier) for headphone with 41 level volume control(volume update with zero-cross detection), traditional mode and direct drive mode, both with anti-pop circuit
- DAC supports sample rate 192k/96k/48k/32k/24k/16k/12k/8k/88.2k/44.1k/ 22.05k /11.025k.
- ADC supports sample rate 96k/48k/32k/24k/16k/12k/8k/44.1k/22.5k/11.025k
- Stereo digital microphone supported.
- Configurable high-pass filter with ADC.
- Configurable AGC/Noise Gate unit.
- Stereo, ClassD/ClassAB dual mode amplifier, up to 2.5W when used as ClassD.
- Slave mode I2S, TDM mode only, TX and RX both.
- 2.0/5.1/7.1 channel I2S Receiver and 2.0/4 channel transmitter
- I2S supports sample rate 192k/96k/48k/32k/24k/16k/12k/8k/88.2k/44.1k/ 22.05k/11.025k.

Power Supply Generation

4 DC-DC

- DC-DC Buck Converter (0.7~1.4V, Up to 1200mA) (DC1)
- DC-DC Buck Converter (1.3~2.2V, Up to 1000mA) (DC2)
- DC-DC Buck Converter (2.6~3.3V, Up to 1200mA, when working without inductance in LDO mode, up to 800mA) (DC3)
- DC-DC Boost Converter (3.0~5.5V, 800mA with external MOSFET) (DC4)

12 LDO and 2 SWITCH:

- LDO voltage regulators (2.6~3.3V,400mA), high PSRR (LDO1)
- LDO voltage regulators (2.6~3.3V,200mA), high PSRR (LDO2)
- LDO voltage regulator (1.5-2.0V, 250mA) (LDO3)
- LDO voltage regulators (2.8~3.5V,400mA), high PSRR (LDO4)
- LDO voltage regulators (2.6~3.3V,150mA), high PSRR (LDO5)
- LDO voltage regulator (0.7~1.4V, 200mA), high PSRR (LDO6)
- LDO voltage regulator (1.5-2.0V, 200mA), high PSRR (LDO7)
- LDO voltage regulators (2.3V - 3.3V, 150mA) , high PSRR (LDO8)
- LDO voltage regulator (1.0~1.5V, 150mA) , high PSRR (LDO9)
- LDO voltage regulator (2.3~3.3V, 100mA) , high PSRR (LDO10)

- LDO voltage regulator (1.5~2.0V, 5mA), for RTC use (LDO11)
- LDO voltage regulator (2.6~3.3V, 15mA), for standby use (LDO12)
- Two SWITCH, configurable to LDO mode
- Over-voltage, Over-current, Over-temperature protection of DC-DCs and LDOs

Battery Charger

- Single-cell Li-battery charger
- Thermal protection for charge control;
- A backup battery charger

Power saving mode

- Several power saving mode including standby mode, sleep mode and deep-sleep mode.
- "Always on" RTC with wake-up alarm
- In deep-sleep with RTC always on, the current of Ibat can be less than 20uA

Ethernet PHY

- RMII interface support with 50MHz reference clock output to MAC
- SMII interface support with 125MHz reference clock output to MAC
- Single-chip 10Base-T and 100Base-TX physical layer solution
- Fully compliant to 100BASE-TX/10BASE-T standards (IEEE 802.3u, FDDI-TP-PMD, and IEEE 802.3)
- Supports two multi-functional LED output
- Supports the full-duplex and half-duplex modes
- Supports Auto-MDIX for detection and correction with the MDI/MDIX auto-crossover function

System Control

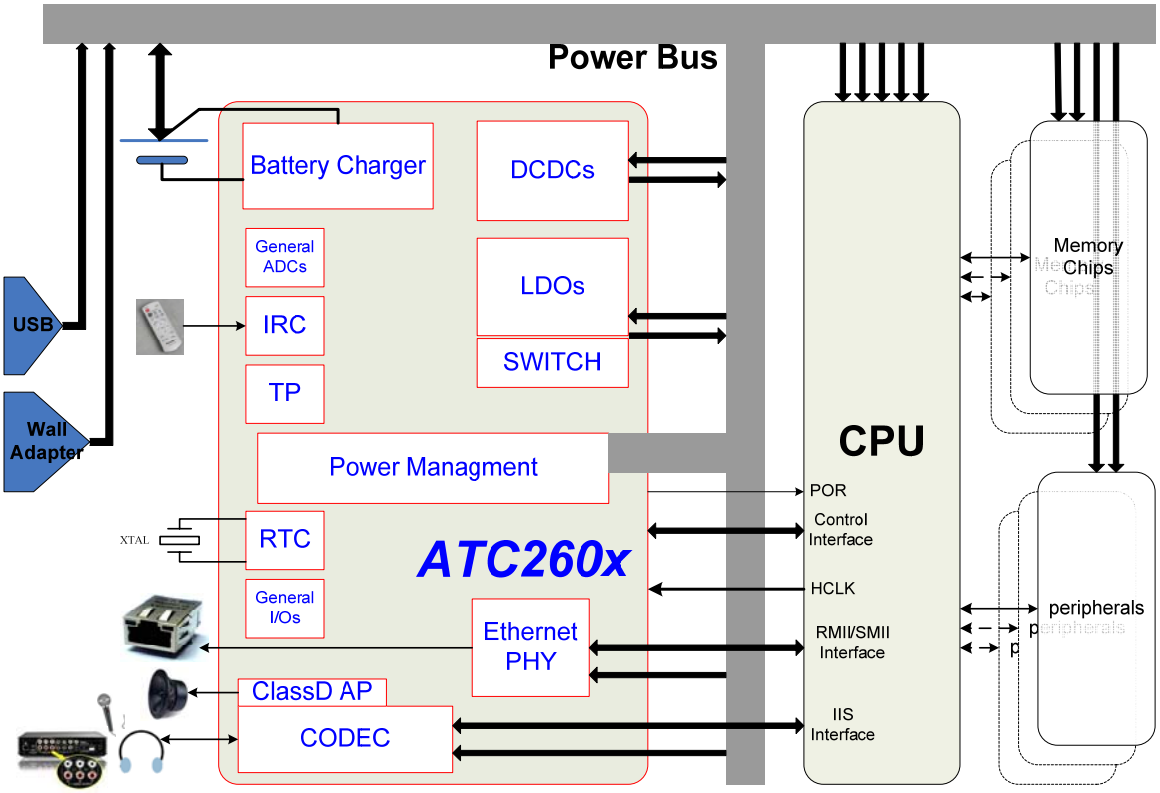
- SPI slave Interface
- Handles power sequencing, power-on reset signal, sleep mode signal and fault conditions interrupt signal
- Adaptive power distribute system, autonomous power source selection (battery, wall adaptor or USB bus)

Additional Features

- Resistance Touch Panel with 12-bit resolution ADC, can be used as wake-up source
- A multi-channel 10-bit ADC, can be used as voltage, current measurement or wake-up sources as Romote control.
- An EXTIRQ to Master SOC
- A few configurable GPIO pins
- 24MHz or 25MHz system clock input supported
- ESD Level of HBM can reach 4000V of all IOs
- ATC2605, EPLQFP128 package, 14*14mm, with 0.4mm pin pitch

- ATC2603, QFN68 package, 8*8mm, with 0.4mm pin pitch

4.3 Typical Applications



4.4 Ordering Information

Part Numbers	Package	Size
ATC2605	EPLQFP128	14*14mm
ATC2603	QFN68	8*8mm

4.5 Functions Contrastive List

Features	ATC2605	ATC2603
Package	EPLQFP128	QFN68
DCDC	4	3
LDO	12	9
SWITCH	2	1
CODEC	√	√
CLASS D	2	1
MIC	2	1
HP OUT	√	√
FMIN	√	√
7.1 chanel	√	X
CHARGER	√	√
Ethernet PHY	√	X
Control Interface	4wire SPI	4wire SPI
I2S	6wire	4wire
Resistence TP	√	X
Remote ADC	√	√
General ADC	4	2
RTC	√	√
IR	√	√

5. Absolute Maximum Rating

These absolute maximum ratings are stress ratings, operating at or beyond these ratings can result in permanent damage. Unless otherwise designated all voltages are relative to ground.

Parameter	Symbol	Min	Max	Unit
Ambient Temperature	Tamb	-30	+70	℃
Storage temperature	Tstg	-55	+150	℃
Supply voltage	DCxIN/WALL/VBUS/BAT/SYSPWR	-0.3	6	V
Input Voltage	Digital IO	-0.3	3.6	V
	Analog IO	-0.3	3.6	V

6. Recommended Operating Conditions

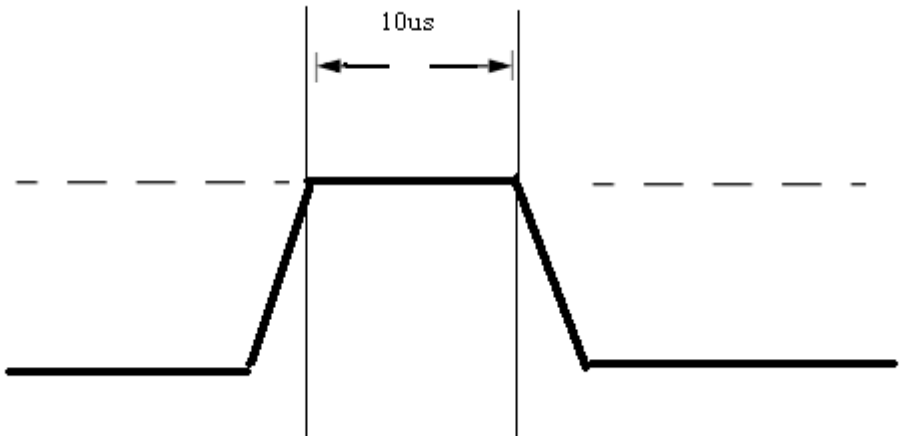
Parameter	Symbol	Min	Typ	Max	Unit
Wall adapter input source	WALL	4		5.5	V
USB VBUS input source	VBUS	4.75		5.25	V
Battery input source	BAT	3		4.2	V
Supply voltage	DC*x*VIN /LDO*x*IN/SW*x*IN	3		5.5	V
Class D supply voltage	CDPVCC*x*	0		5.5	V
Core supply	VDD		1.2		V
IO supply	VCC		3.1		V
Ground	GND/AGND/DC*x*GND/CDPGND*x*		0		V

7. Electronic Characteristics

7.1 Overshoot

The maximum DC voltage on supply power pins is below 6V.

However, during voltage transitions, the device can tolerate overshoot for up to 10us, as shown in Figure below



Parameter	Symbol	Start	Max	Unit
Supply voltage	DcxIN/WALL/VBUS/ BAT	-0.3	8	V

Exposure to overshoot conditions for too many times may affect device reliability. ATC260X can tolerate 1,000 times of such pulses

7.2 Electrostatic Discharge (ESD)

Parameter	Pin	Unit
Human Body Model (HBM)	All	4 KV

7.3 DC Characteristics

3.1V I/Os,

VCC = 3.1V, TA = 0 to 70 °C

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Low-level input voltage	V_{IL}			0.8	V
High-level input voltage	V_{IH}	2.0			V
Low-level output voltage	V_{OL}			0.4	V
High-level output voltage	V_{OH}	2.4			V

2.5V I/O s,

VDDR = 2.5V, TA = 0 to 70 °C

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Low-level output voltage	V_{OL}			0.4	V
High-level output voltage	V_{OH}	2.0			V

8. Control Interface & Register Mapping

8.1 Control Interface

All Functions in ATC260x should be accessed thought a standard SPI interface, configure into the registers or get information.

It supported SPI slave mode 3 only, and the bit rate is up to 10 Mbps.

There are 15 bits transmitted for address with 12bits register address and 3bits reserved (do not care), 16 bits for data, and 1 bit indicate the W/R signal of the register need be accessed.

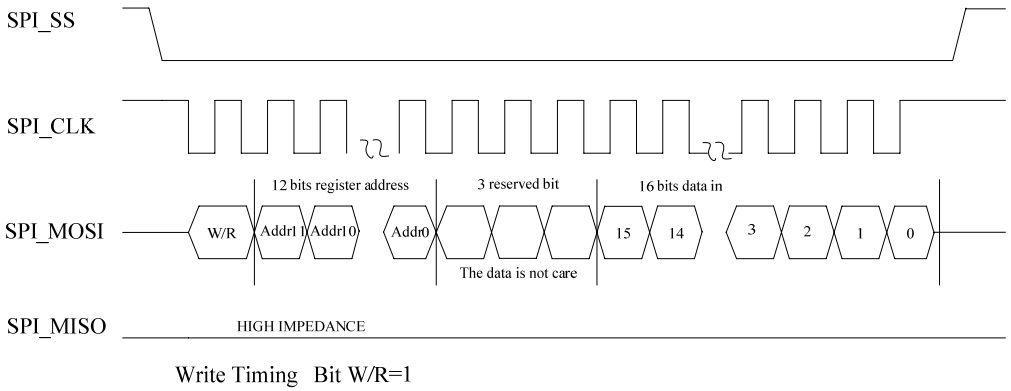


Figure 0-1 SPI write timing

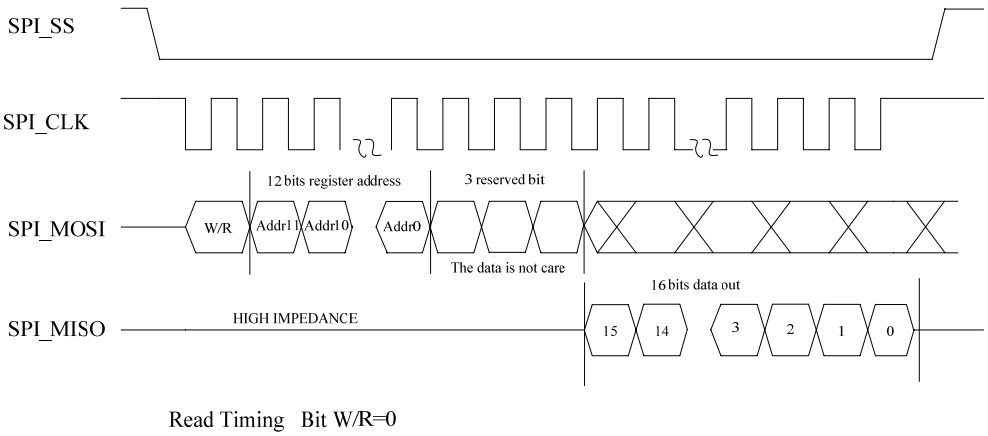


Figure 0-2 SPI read timing

8.2 Register Mapping

15 bits transmitted for address of the register need be accessed. The address mapping of these registers is described as follow:

Start	End	Size(12bit)	Function Module
0x0000	0x0FF	0x100	PMU
			AUX ADC
			RTC
			IRC
0x0100	0x1FF	0x100	CMU
0x0200	0x2FF	0x100	INTS
0x0300	0x3FF	0x100	MFP
0x0400	0x4FF	0x100	AUDIO
0x0500	0x5FF	0x100	Ethernet PHY
0x0600	0x6FF	0x100	TP Controller
0x0700	0xFFF	0x900	Reserved

9. Clocking

A 32.768KHz crystal oscillator should be supplied to ATC260x system to get an accuracy clock for real time clock (RTC) and an alarm function capable of waking up the system. If the clock requirement is not so accurate, an internel oscillator is build in for self use

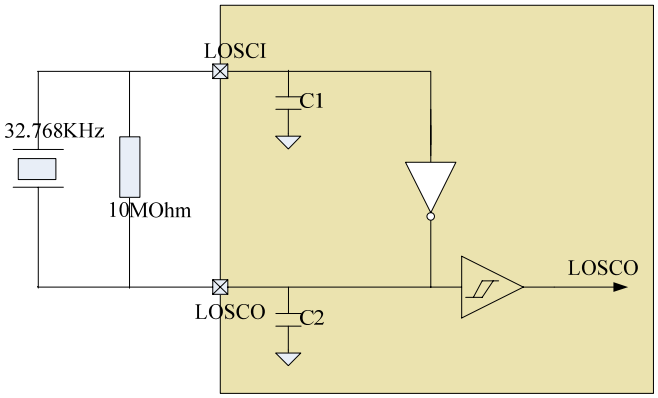


Figure LOSC block diagram (RTCVDD)

The master clock of ATC260x operation can be input directly by the CPU clock output or generated by an external crystal oscillator, 24MHz or 25MHz.

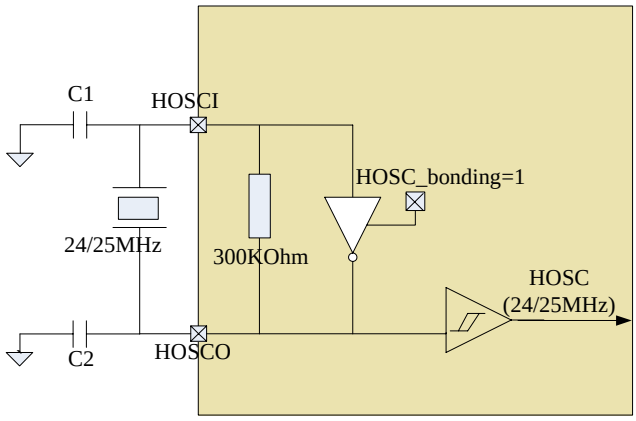


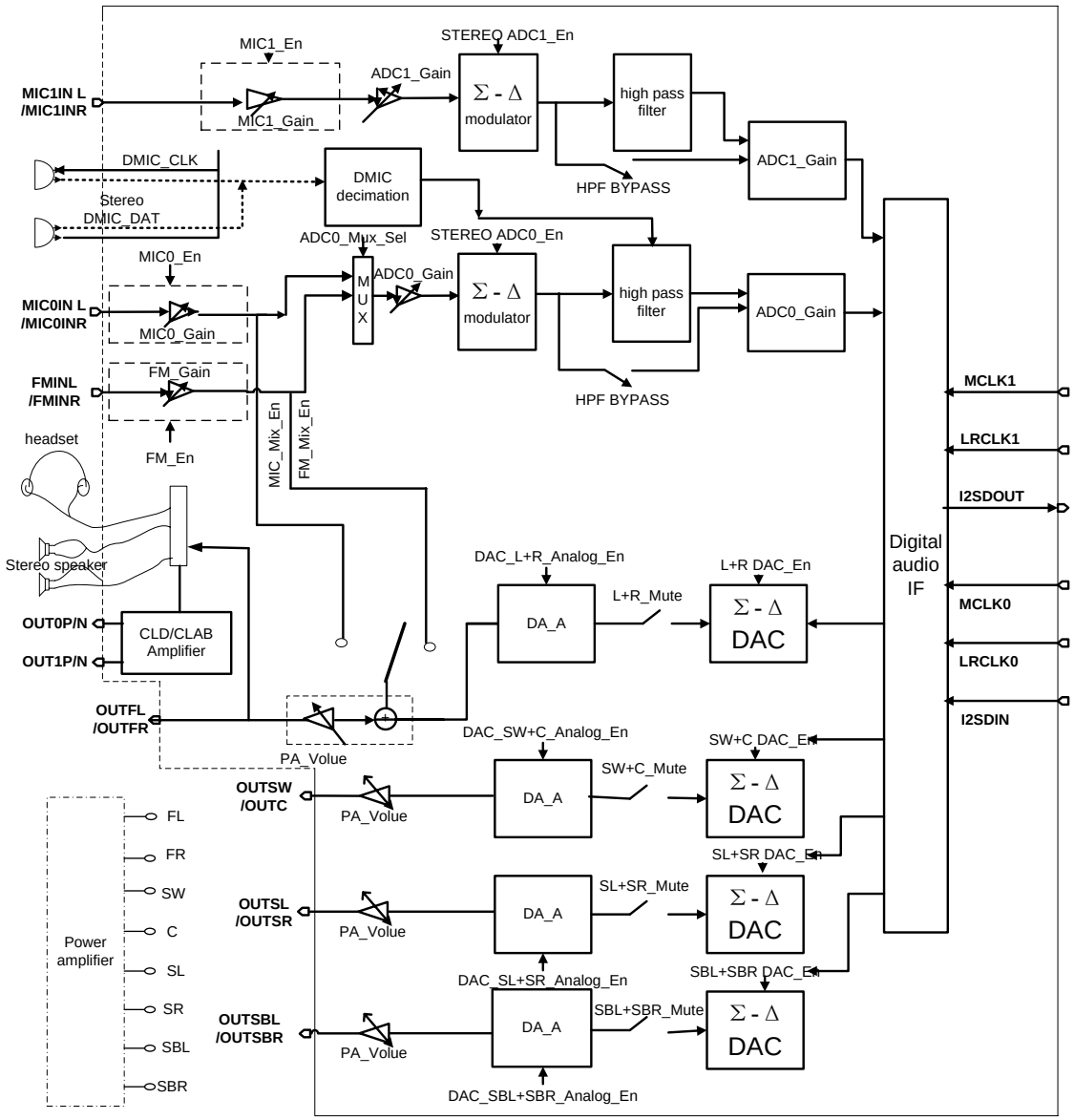
Figure HOSC block diagram (AVCC)

10. Audio Codec Subsystem

10.1 Features

- The Audio Codec subusystem include I2S interface, DAC, ADC, and CLASSD/CLASSAB AP.
- Slave mode I2S, TDM mode only, TX and RX both.
- 2.0/5.1/7.1 channel I2S Receiver and 2.0/4 channel transmitter
- I2S supports sample rate 192k/96k/48k/32k/24k/16k/12k/8k/88.2k/44.1k/ 22.05k/11.025k.
- 7.1 channel DAC, SNR (A-WEIGHTING)>98dB, THD<-80dB. DAC supports sample rate 192k/96k/48k/32k/24k/16k/12k/8k/88.2k/44.1k/ 22.05k /11.025k.
- Stereo 20mW PA (Power Amplifier) for headphone with 41 level volume control(volume update with zero-cross detection), traditional mode and direct drive mode, both with anti-pop circuit
- Two stereo ADCs, SNR (A-WEIGHTING)>91dB, THD<-82dB, for Supporting multi channels DV microphone recording, difference or single-ended input both supported.
- ADC supports sample rate 96k/48k/32k/24k/16k/12k/8k/44.1k/22.5k/11.025k
- Stereo digital microphone supported.
- Configurable high-pass filter with ADC.
- Configurable AGC/Noise Gate unit.
- Stereo, ClassD/ClassAB dual mode amplifier, up to 2.5W when used as ClassD.

10.2 Audio Diagram & Signal Path



10.3 Audio Electronic Characteristics

Test condition:
AVCC=2.9V, VCC=3.1V, VDD=AVDD=Vref= 1.5V, CDPVCC=5V.
When testing DAC+PA or PA，a 16 or 32 ohm load should be included，and when testing CLASSD/CLASSAB，a 4 ohm load should be included.

10.3.1 DAC+PA

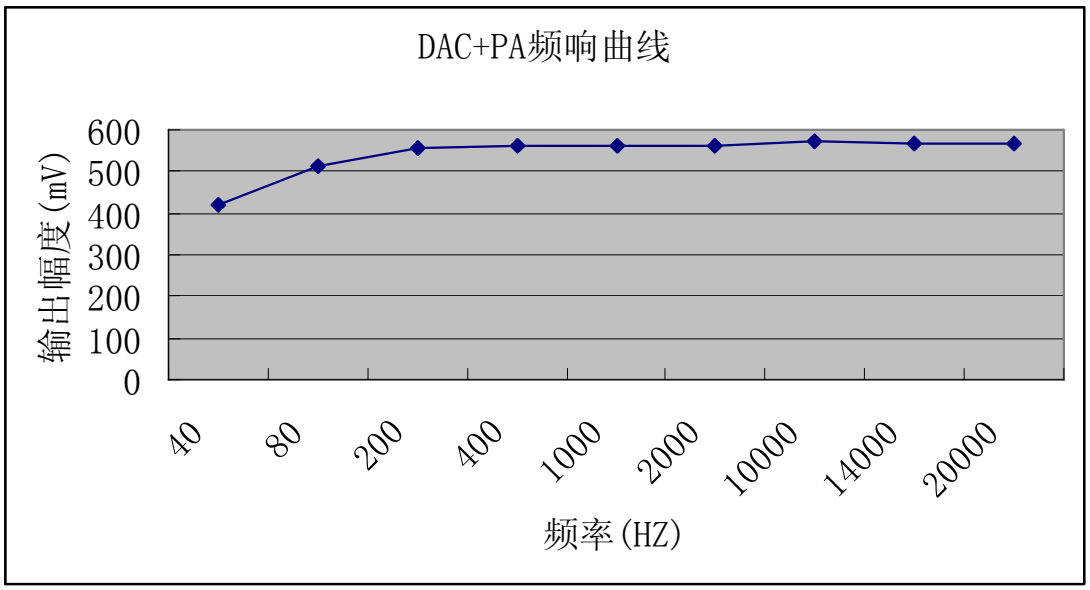
DAC + direct drive PA：

Characteristics	MIN	TYP	MAX	UNIT
Noise		9.6		uV
SNR		94		dB
SNR(A-Weighting)		97.8		dB
Dynamic Range (-48dB Input)		92.7		dB
Dynamic Range (A-Weighting, -48dB Input)		96		dB
THD+N (0dB Input)		-80		dB
Max Ampl (0dB Input)		576		mV
Max Power		20.2		mW
Interchannel Isolation (1k,0dB Input)		-80/-81 (Lmute/Rmute)		dB

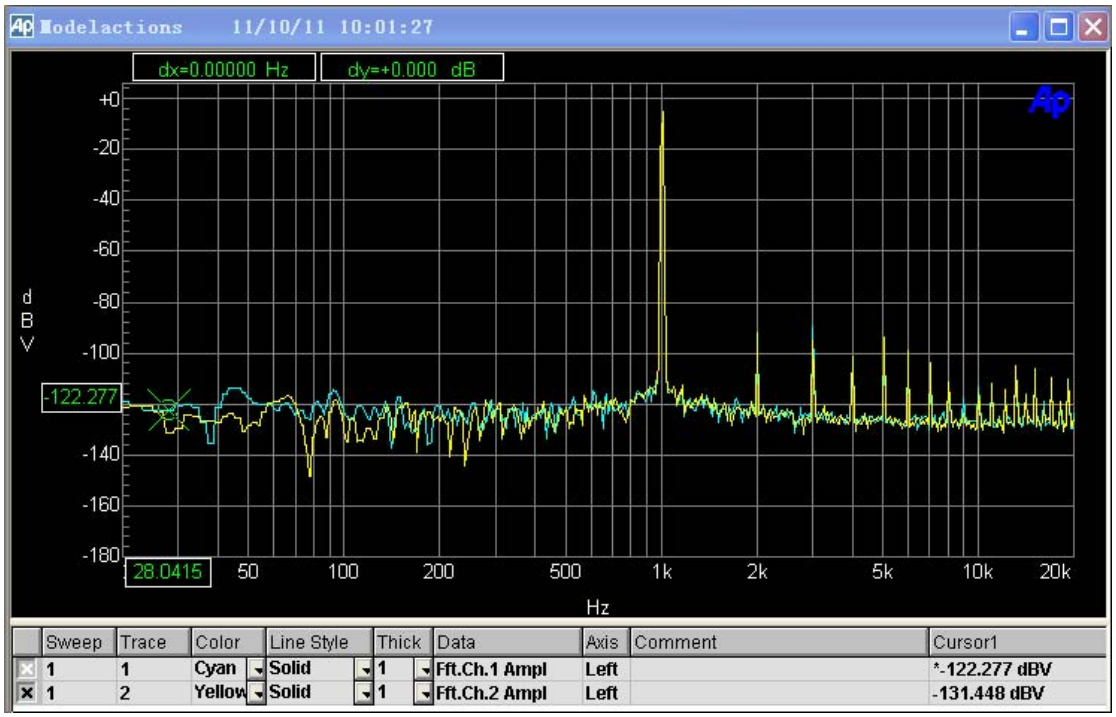
DAC + non direct drive PA：

Characteristics	MIN	TYP	MAX	UNIT
Noise		10		uV
SNR		95		dB
SNR(A-Weighting)		97.4		dB
Dynamic Range (-48dB Input)		93.6		dB
Dynamic Range (A-Weighting, -48dB Input)		96.5		dB
THD+N (0dB Input)		-82		dB
Max Ampl (0dB Input)		563		mV
Max Power		19.22@220uF		mW
Interchannel Isolation (1k,0dB Input)		-78/-78 (Lmute/Rmute)		dB

Frequency Response:



FFT:

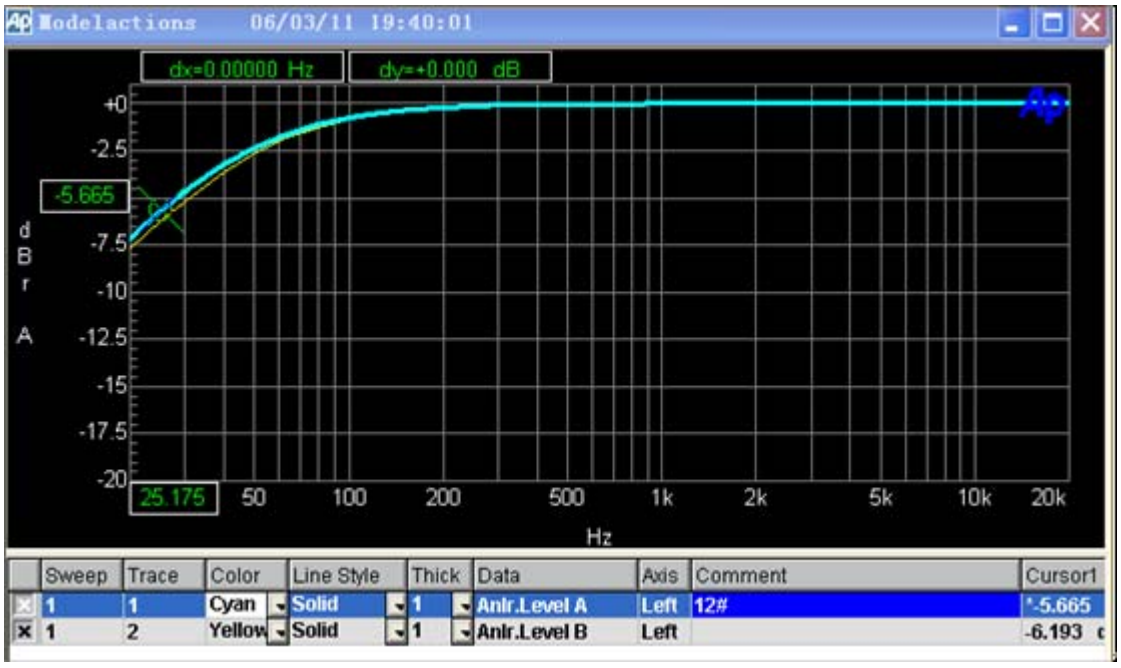


10.3.2 PA

Non Direct Drive PA

Characteristics	MIN	TYP	MAX	UNIT
Noise		11.2		uV
SNR		95		dB
Dynamic Range		93.7		dB
Total Harmonic Distortion+Noise		-85		dB
Output Common Mode Voltage		1.506		Vrms
Full Scale Output Voltage@-60dB thd+n		0.638Vrms (1.958Vpp input)		Vrms
Output Power @16.5ohm		25.3		mW

Frequency Response:

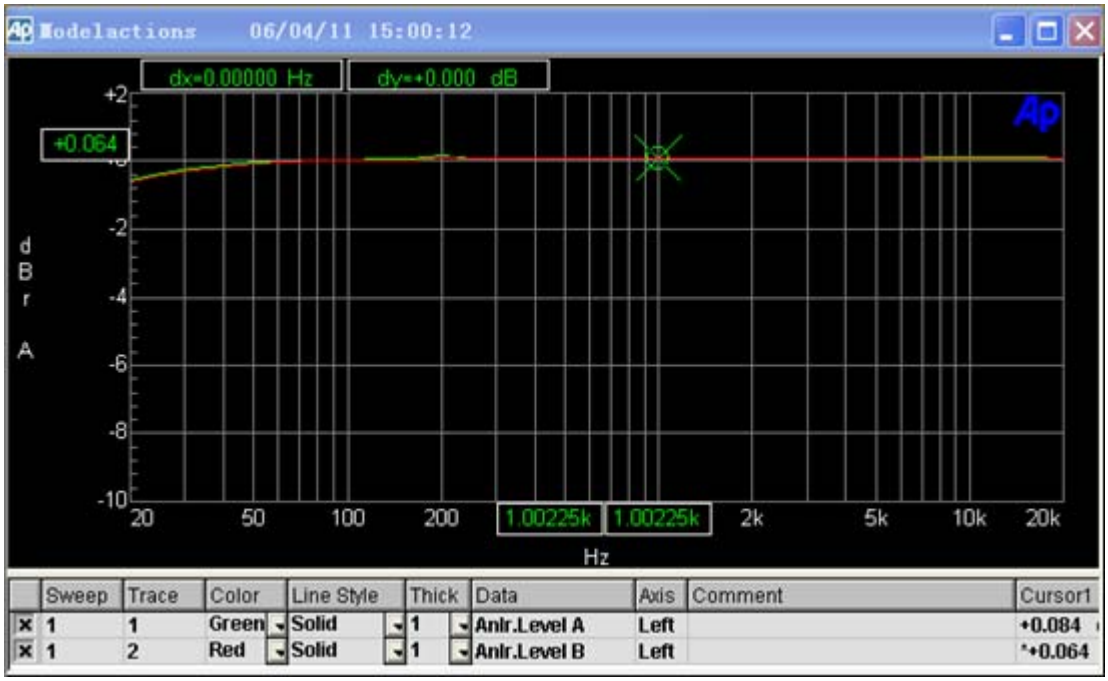


THD+N VS INPUT AMP Curve

Direct Drive PA

Characteristics	MIN	TYP	MAX	UNIT
Noise		12		uV
SNR		94.4		dB
Dynamic Range		93		dB
Total Harmonic Distortion+Noise		-84		dB
Output Common Mode Voltage		1.506/1.506/1.510 （AL/AR/VRO）		Vrms
Full Scale Output Voltage@-60dB thd+n		0.636Vrms (@1.913Vpp)		Vrms
Output Power @16ohm		25.3		mW

Frequency Response:



THD+N VS INPUT AMP Curve

10.3.3 ADC

Dynamic Range (–40 dBFS Input)		89.6@48k		dB
Total Harmonic Distortion+Noise		85.5@48k		dB

10.3.4 CLASSD/CLASSAB

CLASSD@5V:

Characteristics	MIN	TPY（CLD1/CLD2）	MAX	UNIT
SNR		83.3		dB
SNR(A-Weighting)		86.3		dB
THD+N (1W)		-72		dB
Max Power (-20dB THD)		2.3		W
Max Power (-40dB THD)		1.87		W
Effectiency (2.3W)		78		%

CLASSDAB@5V：

Characteristics	MIN	TYP（CLAB1/CLAB2）	MAX	UNIT
SNR		81		dB
SNR(A-Weighting)		83.5		dB
THD+N (500mW)		-70/-70		dB
Max Power (-20dB THD)		0.98		W
Max Power (-40dB THD)		0.74		W
Effectiency (MAX W)		44.8%		%

10.4 Register List

Table 0-1 AUDIO OUT Controller Registers Address

Name	Base Address
AUDIO_IN_OUT_Register	0x0400

Table DAC/PA/IIS/CLASSD Registers

Offset	Register Name	Description
0x00	AUDIOINOUT_CTL	AUDIO IN/OUT Control for I2S Register
0x02	DAC_FILTERCTL0	DAC Control for DAC Filter SAMPLE RATE Register
0x03	DAC_FILTERCTL1	DAC Control for Digital Filter bandwidth Register
0x04	DAC_DIGITALCTL	DAC Control EN&MUTE Register
0x05	DAC_VOLUMECTL0	DAC FL&FR VOLUME Control Register
0x06	DAC_VOLUMECTL1	DAC SW&C VOLUME Control Register
0x07	DAC_VOLUMECTL2	DAC SL&SR VOLUME Control Register
0x08	DAC_VOLUMECTL3	DAC SBL&SBR VOLUME Control Register
0x09	DAC_ANALOG0	DAC Analog 0 Register
0x0a	DAC_ANALOG1	DAC Analog 1 Register
0x0e	CLASSD_CTL0	Class D Control 0 Register
0x0f	CLASSD_CTL1	Class D Control 1 Register
0x10	CLASSD_CTL2	Class D Control 2 Register
0x11	ADC0_DIGITALCTL	ADC0 Digital Control Register
0x12	ADC0_HPFCTL	ADC0 High Pass Filter Control Register
0x13	ADC0_CTL	ADC0 control register
0x14	AGC0_CTL0	AGC0 Control 0 Register
0x15	AGC0_CTL1	AGC0 Control 1 Register
0x16	AGC0_CTL2	AGC0 Control 2 Register
0x17	ADC_ANALOG0	ADC Analog 0 Register
0x18	ADC_ANALOG1	ADC Analog 1 Register
0x19	ADC1_DIGITALCTL	ADC1 Digital Control Register
0x1A	ADC1_CTL	ADC1 Control Register
0x1B	AGC1_CTL0	AGC1 Control 0 Register
0x1C	AGC1_CTL1	AGC1 Control 1 Register
0x1D	AGC1_CTL2	AGC1 Control 2 Register

10.5 Register Description

AUDIOINOUT_CTL

AUDIO IN/OUT Control for I2S Register

Offset = 0x00

Bit(s)	Name	Description	R/W	Reset
15 ：	—	Reserved	RW	0

13				
12	EIDR	Earphone Input Detect IRQ 0: disable 1: enable	RW	0
11	MDD	MCLK Divided to DAC 0:DIV=1 1:DIV=2	RW	0
10	OHSCIEN	Class D overheat or short circuit warning IRQ enable 0: disable 1: enable This bit when enable will enable an interrupt signal to the interrupt controller, while CLASSD_CTL0 bit 5 and bit 6 are enable，and CLASSD_CTL2 bit 12～15 is pulled high.	RW	0
9	OCIEN	Direct Drive Output Over Current status IRQ 1: enable 0: disable This bit when enable will enable an interrupt signal to the interrupt controller, while DAC_ANALOG2 bit5 enable and DAC_ANALOG3 bit8 pulls high.	RW	0
8	OEN	I2S Output Enable. 0: Disable 1: Enable	RW	0
7	OMD	I2S_OUTPUT MODE: 0: 2.0-Channel Mode 1: 4-Channel TDM Mode A Note：In 2.0 -Channel Mode, when adc0 is enable, the output 2 channel of I2S tx is adc0 L and R channel. When adc1 is enable, the output 2 channel of I2S tx is adc1 L and R channel. In 4.0 -Channel Mode, adc0 and adc1 all must be enable, the output 4 channel of I2S tx is adc0L, adc0R, adc1L, adc1R.	RW	0
6:5	IMS	I2S RX&TX Mode Select 00：3 wires mode 01：4 wires mode 10：6 wires mode 11：Reserved	RW	00
4	LB	I2S Loop Back Enable: 0: Disable 1: Enable	RW	0

3:2	IMD	I2S_INPUT MODE: 00: 2.0-Channel Mode 01: 5.1-Channel TDM Mode A 10: 7.1-Channel TDM Mode A 11：Reserved	RW	00
1	INEN	I2S Input Enable. 0: Disable 1: Enable	RW	0
0	—	Reserved	RW	0

DAC_FILTERCTL0

DAC Control for DAC Filter SAMPLE RATE Register

Offset = 0x02

Bit(s)	Name	Description	R/W	Reset
15:13	-	Reserved	R	0
12	DEDSBL&SBR	DACSBL&SBR EN_DITH 1:ENABLE 0:DISABLE	RW	0
11	DEDSL&SR	DACSL&SR EN_DITH 1:ENABLE 0:DISABLE	RW	0
10	DEDSW&C	DACSW&C EN_DITH 1:ENABLE 0:DISABLE	RW	0
9	DEDFL&FR	DACFL&FR EN_DITH 1:ENABLE 0:DISABLE	RW	0
8	DISRS	DAC INPUT SAMPLE RATE SEL 0:MCLK/256 1:MCLK/128	RW	0
7:6	DOSRSSBL&SBR	DAC SBL&SBR OUTPUT SAMPLE RATE SEL 00:MCLK/16 01:MCLK/8 10:MCLK/4 11:MCLK/2	RW	00
5:4	DOSRSSL&SR	DAC SL&SR OUTPUT SAMPLE RATE SEL 00:MCLK/16	RW	00

		01:MCLK/8 10:MCLK/4 11:MCLK/2		
3:2	DOSRSSW&C	DAC SW&C OUTPUT SAMPLE RATE SEL 00:MCLK/16 01:MCLK/8 10:MCLK/4 11:MCLK/2	RW	00
1:0	DOSRSFL&FR	DAC FL&FR OUTPUT SAMPLE RATE SEL 00:MCLK/16 01:MCLK/8 10:MCLK/4 11:MCLK/2	RW	00

Note: in DA_D test mode, DAC OUTPUT SAMPLE RATE should not be set to “11” (MCLK/2).

DAC_ FILTERCTL1

DAC Control for Digital Filter bandwidth Register

Offset = 0x03

Bit(s)	Name	Description	R/W	Reset
15：8	—	Reserved	R	0
7：6	DBWSBL&SBR	DACSBL&SBR BANDWIDTH 00:WIDE 01:MIDDLE 10:NARROW 11:Reserved	RW	00
5：4	DBWSL&SR	DACSL&SR BANDWIDTH 00:WIDE 01:MIDDLE 10:NARROW 11:Reserved	RW	00
3：2	DBWSW&C	DACSW&C BANDWIDTH 00:WIDE 01:MIDDLE 10:NARROW 11:Reserved	RW	00
1：0	DBWFL&FR	DACFL&FR BANDWIDTH	RW	00

		00:WIDE 01:MIDDLE 10:NARROW 11:Reserved		

DAC_DIGITALCTL

DAC Control EN&MUTE Register

Offset = 0x04

Bit(s)	Name	Description	R/W	Reset
15	DMSBR	DACSBR DIGITAL MUTE 1:MUTE 0:NOT MUTE	RW	0
14	DMSBL	DACSBL DIGITAL MUTE 1:MUTE 0:NOT MUTE	RW	0
13	DMSR	DACSR DIGITAL MUTE 1:MUTE 0:NOT MUTE	RW	0
12	DMSL	DACSL DIGITAL MUTE 1:MUTE 0:NOT MUTE	RW	0
11	DMC	DACC DIGITAL MUTE 1:MUTE 0:NOT MUTE	RW	0
10	DMSW	DACSW DIGITAL MUTE 1:MUTE 0:NOT MUTE	RW	0
9	DMFR	DACFR DIGITAL MUTE 1:MUTE 0:NOT MUTE	RW	0
8	DMFL	DACFL DIGITAL MUTE 1:MUTE 0:NOT MUTE	RW	0
7	DESBR	DACSBR DIGITAL ENABLE 1:ENABLE 0:DISABLE	RW	0
6	DESBL	DACSBL DIGITAL ENABLE	RW	0

		1:ENABLE 0:DISABLE		
5	DESR	DACSR DIGITAL ENABLE 1:ENABLE 0:DISABLE	RW	0
4	DESL	DACSL DIGITAL ENABLE 1:ENABLE 0:DISABLE	RW	0
3	DEC	DACC DIGITAL ENABLE 1:ENABLE 0:DISABLE	RW	0
2	DESW	DACSW DIGITAL ENABLE 1:ENABLE 0:DISABLE	RW	0
1	DEFR	DACFR DIGITAL ENABLE 1:ENABLE 0:DISABLE	RW	0
0	DEFL	DACFL DIGITAL ENABLE 1:ENABLE 0:DISABLE	RW	0

DAC_ VOLUMECTLO

DAC FL&FR VOLUME CONTROL (3/8 dB/level)

Offset = 0x5

Bit(s)	Name	Description	R/W	Reset
15:8	DACFR_VOLUME	VOLUME CONTROL 3/8 dB/level FFH ： +24 dB …… BFH : 0 dB BEH : -3/8 dB …… 00H : -72 dB	RW	BE

7:0	DACFL_VOLUME	VOLUME CONTROL 3/8 dB/level FFH ： +24 dB …… BFH : 0 dB BEH : -3/8 dB …… 00H : -72 dB	RW	BE

DAC_ VOLUMECTL1

DAC SW&C VOLUME CONTROL (3/8 dB/level)

Offset = 0x6

Bit(s)	Name	Description	R/W	Reset
15:8	DACC_VOLME	VOLUME CONTROL 3/8 dB/level FFH ： +24 dB …… BFH : 0 dB BEH : -3/8 dB …… 00H : -72 dB	RW	BE
7:0	DACSW_VOLUME	VOLUME CONTROL 3/8 dB/level FFH ： +24 dB …… BFH : 0 dB BEH : -3/8 dB …… 00H : -72 dB	RW	BE

DAC_ VOLUMECTL2

DAC SL&SR VOLUME CONTROL 3/8 dB/level

Offset = 0x7

Bit(s)	Name	Description	R/W	Reset

15:8	DACSR_VOLME	DAC6_VOLME CONTROL 3/8 dB/level FFH ： +24 dB …… BFH : 0 dB BEH : -3/8 dB …… 00H : -72 dB	RW	BE
7:0	DACSL_VOLME	DAC5_VOLME CONTROL 3/8 dB/level FFH ： +24 dB …… BFH : 0 dB BEH : -3/8 dB …… 00H : -72 dB	RW	BE

DAC_ VOLUMECTL3

DAC SBL&SBR VOLUME CONTROL 3/8 dB/level

Offset = 0x8

Bit(s)	Name	Description	R/W	Reset
15:8	DACSBR_VOLME	DAC8_VOLME CONTROL 3/8 dB/level FFH ： +24 dB …… BFH : 0 dB BEH : -3/8 dB …… 00H : -72 dB	RW	BE
7:0	DACSBL_VOLME	DAC7_VOLME CONTROL 3/8 dB/level FFH ： +24 dB …… BFH : 0 dB BEH : -3/8 dB …… 00H : -72 dB	RW	BE

DAC_ANALOG0

DAC Analog Register
Offset = 0x9

Bit(s)	Name	Description	R/W	Reset
15:4	--	Reserved	R	010100110101
3	KFEN	Karaoke Mix Function Enable 0：disable 1：enable Note ： when enable this bit, MIC0INL and MIC0INR will be added and transmitted to PA	RW	0
2:0	--	Reserved	R	101

DAC_ANALOG1

DAC Analog Register
Offset = 0xA

Bit(s)	Name	Description	R/W	Reset
15	MICMUTE	MIC mute, 0: mute 1: not mute	RW	0
14	FMMUTE	FM mute, 0: mute 1: not mute	RW	0
13	DACSBL&SBRMUTE	DACSBL&SBR Playback Mute 0: mute DAC Playback, 1: enable DAC playback	RW	0
12	DACSL&SRMUTE	DACSL&SR Playback Mute 0: mute DAC Playback, 1: enable DAC playback	RW	0
11	DACSW&CMUTE	DACSW&C Playback Mute 0: mute DAC Playback, 1: enable DAC playback	RW	0
10	DACFL&FRMUTE	DACFL&FR Playback Mute 0: mute DAC Playback,	RW	0

		1: enable DAC playback		
9:6	--	Reserved	R	000
5:0	Volume	Headphone Amp Volume Control. Total 41 level (Values between 000000b and 101000b are valid. Any value over 101000b set to it will be taken as 101000b actually. Reading value will just show what you have written to it.)	RW	000000

CLASSD_CTL0

Class D Control 0 Register

Offset = 0xE

Bit(s)	Name	Description	R/W	Reset
15:13	OTPR	Over temperature protect Range 000: 103 / 65 deg 001: 114 / 72 deg 010: 125 / 77 deg 011: 138 / 84 deg 100: 147 / 89 deg 101: 158 / 94 deg 110: 170 / 99 deg 111: 190 / 104 deg	RW	100
12:11	GAIN	Gain select 00: 12dB 01: 18dB 10: 24dB 11: 30dB	RW	00
10	DBGIN	Debug mode , input H or L to power stage 1: input H, power stage output L 0: input L ,power stage output H	RW	0
9	NCLPEN	Non-Clip enable 1:enable 0:disable	RW	0
8	SABD	Internal mode select 1:Class AB mode 0:Class D mode	RW	0

7	SSEN	Spread-Spectrum enable 1: enable 0: disable	RW	0
6	SCEN	Short-Circuit protection enable 1: enable 0: disable	RW	0
5	OTPEN	Over temperature protection enable 1:enable 0:disable	RW	0
4	FBEN	Feedback enable 1: enable 0: disable	RW	0
3	PEN	Power stage enable 1: enable 0: disable	RW	0
2	MUTE	Mute Class D output 1: no mute 0: mute	RW	0
1	CLD2EN	Class D2 enable 1: enable 0: disable	RW	0
0	CLD1EN	Class D1 enable 1: enable 0: disable	RW	0

CLASSD_CTL1

Class D Control 1 Register

Offset = 0xF

Bit(s)	Name	Description	R/W	Reset
15:12	——	(For analog future use)	RW	0000
11:10	SSR	Spread-Spectrum Range 00:500~530K 3% 01:500~564K 6% 10:500~600K 9% 11:500~636K 12%	RW	01
9:8		Fix switch Freq. select 00:385kHz	RW	00

	FSEN	01:450kHz 10:600kHz 11:750kHz		
7:6	NCLPR	Non-Clip Range 00: 16Cycle clipping 01: 32Cycle clipping 10:48 Cycle clipping 11:64 Cycle clipping	RW	01
5:4	EDG	Output rise/fall edge 00:5ns 01:10ns 10:20ns 11:30ns	RW	01
3:0	IBREG	Class D bias current select 0000：2uA 0001：0.5uA 0010：1uA 0100：4uA 1000：8uA （other value is added by above. eq. Set 0011, means 0.5uA+1uA=1.5uA）	RW	0000

CLASSD_CTL2

Class D Control 2 Register
Offset = 0x10

Bit(s)	Name	Description	R/W	Reset
15	OHWN2	Class D 2 Overheat warning state 0: normal 1: overheat	R	0
14	SCWN2	Class D 2 Short Circuit warning state 0: normal 1: short circuit	R	0
13	OHWN1	Class D 1 Overheat warning state 0: normal 1: overheat	R	0
12	SCWN1	Class D 1 Short Circuit warning state 0: normal	R	0

		1: short circuit		
11:9	ATIME	Non-Clip Attack time select 000: 0.26ms/dB 001: 0.5ms/dB 010: 1.0ms/dB 011: 2.0ms/dB 100: 4.1ms/dB 101: 8.2ms/dB 110: 16.4ms/dB 111: 32.8ms/dB	RW	011
8:6	RTIME	Non-Clip Release time select 000: 16.4ms/dB 001: 32.8ms/dB 010: 0.07s/dB 011: 0.13s/dB 100: 0.26s/dB 101: 0.52s/dB 110: 1.05s/dB 111: 2.1s/dB	RW	011
5:4	VREC[1：0]	Soft-clip recovery voltage / Pout @ 4ohm 00: 1.8v , 180mW 01: 1.85v, 245mw 10: 1.9v, 320mw 11: 1.95v, 405mW	RW	01
3:0	Reserved	Reserved	RW	0000

ADC0_DIGITALCTL

ADC0 Digital Control Register

Offset=0x11

Bits	Name	Description	RW	Reset
15:12	-	Reserved	R	0
11	AD0LR	ADC0L And ADC0R Added enable 0: disable1: enable Note：this bit is designed for karaoke use，when this Bit is “1”; ADC0L data and ADC0R data are added and transformed to MCU	RW	0

10	AD0DEN	ADC0 Digital Debug Enable 0: disable 1: enable	RW	0
9:6	ADGC0	ADC0 DIGITAL Gain Control 0000: 0dB 0001: 3dB 0010: 6dB 0011: 9dB 0100: 12dB 0101: 15dB 0110: 18dB 0111: 21dB 1000: 24dB 1001: 27dB 1010: 30dB 1011: 33dB 1100: 36dB 1101: 39dB 1110: 42dB 1111: 45dB	RW	0000
5	DCD	DMIC CLOCK Divide 0: div＝4 1: div＝2 (for voice recording)	RW	0
4	DCEN	DMIC CLOCK enable 0: disable 1: enable	RW	0
3	VREN	Voice Recording enable 0: disable 1: enable NOTE: when voice recording is enable, bit 5 should be set to “1”.	RW	0
2	DRFS	DMIC Rising or falling edge sampling Select 0: Left channel ： sampling at rising edge， Right channel： sampling at falling edge； 1: Left channel: sampling at falling edge， Right channel: sampling at rising edge；	RW	0
1	MLEN	DMIC Left filter enable 0: disable 1: enable	W	0
0	DMREN	DMIC Right filter enable	RW	0

		0: disable 1: enable		

Note: when DMIC is enable, ADC0 should be disable, and when ADC0 is enable, DMIC should be disable. That is to say, when ADC0_DIGITALCTL bit [0] or bit [1] is “1”, ADC0_CTL bit [2] and bit [3] both should be set to “0”, when ADC0_CTL bit [2] or bit [3] is “1”, ADC0_DIGITALCTL bit [0] and bit [1] both should be set to “0”. When DMIC left filter is enabled, the output of DMIC right filter is zero, on the other hand, when DMIC right filter is enabled, the output of DMIC left filter is zero.

ADC0_HPFCTL

ADC0 Digital Control Register
Offset=0x12

Bits	Name	Description	RW	Reset
15:8	-	Reserved	R	0
7:6	SRSEL0	SR select for removing wind noise filter0 00:8K/11.025K/12K 01:16K/22.05K/24K 10:32K/44.1K/48K 11:Reserved	RW	00
5:3	WNHPF0CUT	For Wind Noise filter0 Cut Off frequency, See Figure 2.2.1 for details	RW	000
2	HPF0DW	Select High Pass Filter0 for DC offset or Wind Noise 0: for DC offset 1: for Wind Noise	RW	0
1	HPF0LEN	High Pass Filter0 L Enable 0：enable 1：disable	RW	0
0	HPF0REN	High Pass Filter0 R Enable 0：enable 1：disable	RW	0

ADC0_CTL

ADC0 control register
Offset=0x13

Bits	Name	Description	RW	Reset
15	VMICINEN	Internal MIC Power VMIC Control 0：disable 1：enable	RW	0
14	FMLEN	FM input left channel enable; 0: Disable 1: Enable	RW	0
13	FMREN	FM input right channel enable; 0: Disable 1: Enable	RW	0
12:10	FMGAIN	FM input gain control: 000 -3.0db 001 -1.5db 010 0.0db 011 1.5db 100 3.0db 101 4.5db 110 6.0db 111 7.5db	RW	010
9	VMICEXEN	External MIC Power VMIC enabled 0 disabled 1 enabled	RW	0
8:7	VMICEXST	External MIC Power VMIC voltage setting 00 2.7V 01 2.9V 10 3.1V 11 3.2V	RW	01
6	MIC0LEN	MIC0 input L Channel Enabled 0：disable 1：enable	RW	0
5	MIC0REN	MIC0 input R Channel Enabled 0：disable 1：enable	RW	0
4	MIC0FDSE	MIC0 input Fully differential or Single ended select 0 FD; 1 SE;	RW	0
3	AD0LEN	ADC0 Left Channel Enable 0: disable 1: enable	RW	0

2	AD0REN	ADC0 Right Channel Enable 0: disable 1: enable	RW	0
1:0	ADCIS	Sigma-Delta A/D0 Input Select: 00: Select MIC 01: Select FM 10: Select Internal Analog Mixer Output (AOUT) 11: Reserved	RW	01

AGC0_CTL0

AGC0 Control Register 0

Offset = 0x14

格式有问题

Bits	Name	Description	RW	Reset
15:12	AMP1G0L	AMP1 Left Channel Gain Select at AGC0 disabled 0000: 16.5dB 0001: 18dB 0010: 19.5dB 0011: 21dB 0100: 22.5dB 0101: 24dB 0110: 25.5dB 0111: 27dB 1000: 28.5dB 1001: 30dB 1010: 31.5dB 1011: 33dB 1100: 34.5dB 1101: 36dB 1110: 37.5dB 1111: 39dB AMP1 AGC Gain can be Read out when AGC0 is enabled, and can be written and read out when AGC0 is disabled.	RW	1001
11:8	AMP1G0R	AMP1 Right Channel Gain Select at AGC0 disabled 0000: 16.5dB 0001: 18dB 0010: 19.5dB 0011: 21dB 0100: 22.5dB 0101: 24dB 0110: 25.5dB 0111: 27dB 1000: 28.5dB 1001: 30dB 1010: 31.5dB	RW	1001

		1011: 33dB 1100: 34.5dB 1101: 36dB 1110: 37.5dB 1111: 39dB AMP1 AGC Gain can be Read out when AGC0 is enabled, and can be written and read out when AGC0 is disabled.		
7	IMICSHD	Internal MIC Power Controlled by External MIC Plug enable 0：disable 1：enable	RW	0
6:3	-	Reserved for analog future use	RW	0110
2:0	AMP0GR1	AMP1 Gain Boost Range Select 000: +3dB 001: +6dB 010: +9dB 011: +12dB 100: +13.5dB 101: +15dB 110: +16.5dB 111: +18dB	RW	011

AGC0_CTL1

AGC0 Control 1 Register
Offset=0x15

Bits	Name	Description	RW	Reset
15:13	-	Reserved for analog future use	RW	000
12:10	NGT0	AGC0 Noise gate statistic time 000: 4*RMSCY 001: 8*RMSCY(1.36ms) 010: 16*RMSCY 011: 32*RMSCY 100: 64*RMSCY 101: 128*RMSCY 110: 256*RMSCY 111: 512*RMSCY	RW	001

9:7	ATKT0	AGC0 Attack(Gain ramp-down) Time for every Gain step 000: 1*RMSCY 001: 2*RMSCY 010: 4*RMSCY(683us) 011: 8*RMSCY 100: 16*RMSCY 101: 32*RMSCY 110: 64*RMSCY 111: 128*RMSCY	RW	010
6:4	DCYT0	AGC0 Decay(Gain ramp-up) Time for every Gain step 000: 16*RMSCY 001: 32*RMSCY(5.46ms) 010: 64*RMSCY 011: 128*RMSCY 100: 256*RMSCY 101: 512*RMSCY 110: 1024*RMSCY 111: 2048*RMSCY	RW	001
3:2	CMR0	AGC0 RC filter cutoff frequency select 00 :207Hz; 01: 414Hz; 10 : 828Hz; 11 : 1.65kHz;	RW	10
1:0	SCY0	AGC0 sense Cycle select 00 :341us; 01: 683us 10 :1366us; 11 :2732us;	RW	10

AGC0_CTL2

AGC0 Control 2 Register
Offset=0x16

Bits	Name	Description	RW	Reset

15:13	TARGL0	AGC0 AMP1 Target level select at AMP2GR=+6dB 000: -42dBFS 001: -39dBFS 010: -36dBFS 011: -33dBFS 100: -30dBFS 101: -27dBFS 110: -24dBFS 111: -21dBFS	RW	100
12:10	NGTHSEL0	AGC0 Noise Gate Threshold select at +28.5dB Gain（Peak sense） 000: -27dBFS 001: -30dBFS 010: -33dBFS 011: -36dBFS 100: -39dBFS 101: -42dBFS 110: -45dBFS 111: -51dBFS	RW	011
9	MICAAEN	ADC0 MIC to PA Path differential compensation enable 0: Disable 1: Enable	RW	0
8	ADBEN	AGC0 Analog Debug enabled(only for AGC0) 0：disable 1：enable	RW	0
7	RMSINSEL0	AGC0 sense input source select 0 Left 1 Right	RW	0
6	-	Reserved for analog future use	RW	1
5	NGSLEN0	AGC0 Noise Gate maintain current Gain or keep silence 0 maintain current Gain 1 keep silence	RW	0
4	NGTEN0	AGC0 Noise Gate function enabled 0: disabled 1: enabled	RW	0
3	ZEROC0	AGC0 Gain change at zero-cross enabled 0: disabled 1: enabled	RW	0

2	GREN0	AGC0 Gain_con gain reset function enabled 0: disabled 1:enabled	RW	0
1	AGC0LEN	AGC0 Left channel Enabled 0: disabled 1: enabled	RW	0
0	AGC0REN	AGC0 Right channel Enabled 0: disabled 1: enabled	RW	0

ADC_ANALOG0

ADC Analog 0 Register

Offset=0x17

Bits	Name	Description	RW	Default
15:13	IVSRMSTN	IVSRMS bias tune 000 -25% 001 -18.75% 010 -12.5% 011 -6.25% 100 2uA 101 +6.25% 110 +12.5% 111 +18.75%	RW	100
12：8	—	Reserved for analog future use	RW	00010
7：5	OPBC1	The bias current select for OPAD1 in A/D: 000 3uA 001 4uA 010 5uA 011 6uA 100 7uA 101 8uA 100 9 uA 110 10 uA 111 11 uA	RW	011

4:3	OPBC23	The bias current select for OPAD2/3 in A/D: 00 2uA 01 3uA 10 4uA 11 5uA	RW	01
2:0	VRDABC	Audio A/D Voltage Reference bias current select: 000 2uA 001 3uA 010 4uA … 110 8uA 111 9uA	RW	001

ADC_ANALOG1

ADC Analog 1 Register

Offset=0x18

Bits	Name	Description	RW	Default
15:13	LPFBC	Audio A/D LPF bias current select: 000 3uA 001 3.5uA 010 4uA 011 4.5uA 100 5uA 101 5.5uA 110 6uA 111 6.5uA	RW	100
12:11	LPFBUFBC	FD LPF BUF OP bias current select: 00 4uA 01 5uA 10 6uA 11 7uA	RW	01
10	ADCBIAS	ADC Total Bias Tune 0 Normal 1 +50%	RW	0

9:8	—	Reserved for analog future use	RW	01
7:6	FD1BC	MIC Preamp FDOP1 bias current select : 00 3uA 01 4uA 10 5uA 11 6uA	RW	01
5:4	FD2BC	MIC Preamp FDOP2 bias current select : 00 2uA 01 3uA 10 4uA 11 5uA	RW	01
3:2	FD1BUFBC	MIC Preamp FDOP2 bias current select : 00 2uA 01 3uA 10 4uA 11 5uA	RW	01
1:0	FMBC	FM Pre-amplifiers bias current select: 00 3uA 01 4uA 10 5uA 11 6uA	RW	01

ADC1_DIGITALCTL

ADC1 Digital Control 1 Register
Offset=0x19

Bits	Name	Description	RW	Reset
15	AD1LR	ADC1L And ADC1R Added enable 0: disable 1: enable Note：this bit is designed for karaoke use，when this Bit is “1”; ADC1L data and ADC1R data are added and transformed to MCU.	RW	0
14	AD1DEN	ADC1 Digital Debug Enable 0: disable 1: enable	RW	0

13:12	SRSEL0	SR select for removing wind noise filter1 00:48K/24K/12K 01:44.1K/22.05K/11.025K 10:32K/16K/8K 11:Reserved	RW	00
11:9	WNHPF1CUT	High Pass Filter1 For Wind Noise Cut Off frequency See Figure 02-1 for details.	RW	000
8	HPF1DW	Select High Pass Filter1 for DC offset or Wind Noise 0: for DC offset 1: for Wind Noise	RW	0
7	HPF1EN	High Pass Filter1 L Enable 0：enable 1：disable	RW	0
6	HPF1EN	High Pass Filter1R Enable 0：enable 1：disable	RW	0
5:2	ADGC1	ADC1 DIGITAL Gain Control 0000: 0dB 0001: 3dB 0010: 6dB 0011: 9dB 0100: 12dB 0101: 15dB 0110: 18dB 0111: 21dB 1000: 24dB 1001: 27dB 1010: 30dB 1011: 33dB 1100: 36dB 1101: 39dB 1110: 42dB 1111: 45dB	RW	0000
1:0		Reserved	RW	00

ADC1_CTL

ADC1 Control Register

Offset=0x1a

Bits	Name	Description	RW	Reset
15:9	—	Reserved for analog future use	RW	0
8	VRDA0EN	VRDA output0 enable 0 disabled 1 enabled	RW	0
7	VRDA1EN	VRDA output1 enable 0 disabled 1 enabled	RW	0
6:5	—	Reserved for analog future use	RW	00
4	MIC1LEN	MIC1 input L Channel Enabled 0：disable 1：enable	RW	0
3	MIC1REN	MIC1 input R Channel Enabled 0：disable 1：enable	RW	0
2	MIC1FDSE	MIC1 input Fully differential or Single ended select 0 FD; 1 SE;	RW	0
1	AD1LEN	ADC1 L Channel Enable 0：disable 1：enable	RW	0
0	AD1REN	ADC1 R Channel Enable 0：disable 1：enable	RW	0

AGC1_CTL0

AGC1 Control 0 Register
Offset = 0x1b

Bits	Name	Description	RW	Reset

15:12	AMP1G1L	AMP1 Left Channel Gain Select at AGC1 disabled When AMP1GRW=1 0000: 16.5dB 0001: 18dB 0010: 19.5dB 0011: 21dB 0100: 22.5dB 0101: 24dB 0110: 25.5dB 0111: 27dB 1000: 28.5dB 1001: 30dB 1010: 31.5dB 1011: 33dB 1100: 34.5dB 1101: 36dB 1110: 37.5dB 1111: 39Db AMP1 AGC Gain can be Read out when AGC1 is enabled, and can be written and read out when AGC1 is disabled.	RW	1001
11:8	AMP1G1R	AMP1 Right Channel Gain Select at AGC1 disabled When AMP1GRW=1 0000: 16.5dB 0001: 18dB 0010: 19.5dB 0011: 21dB 0100: 22.5dB 0101: 24dB 0110: 25.5dB 0111: 27dB 1000: 28.5dB 1001: 30dB 1010: 31.5dB 1011: 33dB 1100: 34.5dB 1101: 36dB 1110: 37.5dB 1111: 39dB AMP1 AGC Gain can be Read out when AGC1 is enabled, and can be written and read out when AGC1 is disabled.	RW	1001

7:3	-	Reserved for analog future use	RW	00110
2:0	AMP1GR1	AMP1 Gain Boost Range Select 000: +3dB 001: +6dB 010: +9dB 011: +12dB 100: +13.5dB 101: +15dB 110: +16.5dB 111: +18dB	RW	011

AGC1_CTL1

AGC1 Control 2 Register
Offset=0x1c

Bits	Name	Description	RW	Reset
15:13	-	Reserved for analog future use	RW	000
12:10	NGT1	AGC1 Noise gate statistic time 000: 4*RMSCY 001: 8*RMSCY(1.36ms) 010: 16*RMSCY 011: 32*RMSCY 100: 64*RMSCY 101: 128*RMSCY 110: 256*RMSCY 111: 512*RMSCY	RW	001

9:7	ATKT1	AGC1 Attack(Gain ramp-down) Time for every Gain step 000: 1*RMSCY 001: 2*RMSCY 010: 4*RMSCY(683us) 011: 8*RMSCY 100: 16*RMSCY 101: 32*RMSCY 110: 64*RMSCY 111: 128*RMSCY	RW	010
6:4	DCYT1	AGC1 Decay(Gain ramp-up) Time for every Gain step 000: 16*RMSCY 001: 32*RMSCY(5.46ms) 010: 64*RMSCY 011: 128*RMSCY 100: 256*RMSCY 101: 512*RMSCY 110: 1024*RMSCY 111: 2048*RMSCY	RW	001
3:2	CMR1	AGC1 RC filter cutoff frequency select 00 :207Hz; 01: 414Hz; 10 : 828Hz; 11 : 1.65kHz;	RW	10
1:0	SCY1	AGC1 sense Cycle select 00 :341us; 01: 683us 10 :1366us; 11 :2732us;	RW	10

AGC1_CTL2

AGC1 Control 2 Register

Offset=0x1d

Bits	Name	Description	RW	Reset

15:13	TARGL1	AGC1 AMP1 Target level select at AMP2GR=+6dB 000: -42dBFS 001: -39dBFS 010: -36dBFS 011: -33dBFS 100: -30dBFS 101: -27dBFS 110: -24dBFS 111: -21dBFS	RW	100
12:10	NGTHSEL1	AGC1 Noise Gate Threshold select at +28.5dB Gain（Peak sense） 000: -27dBFS 001: -30dBFS 010: -33dBFS 011: -36dBFS 100: -39dBFS 101: -42dBFS 110: -45dBFS 111: -51dBFS	RW	011
9:8	-	Reserved for analog future use	RW	00
7	RMSINSEL1	AGC1 sense input source select 0 Left 1 Right	RW	0
6	-	Reserved for analog future use	RW	1
5	NGSLEN1	AGC1 Noise Gate1 maintain current Gain or keep silence 0 maintain current Gain 1 keep silence	RW	0
4	NGTEN1	AGC1 Noise Gate function enabled 0: disabled 1: enabled	RW	0
3	ZEROC1	AGC1 Gain change at zero-cross enabled 0: disabled 1: enabled	RW	0
2	GREN1	AGC1 gain_con gain reset function enabled 0: disabled 1: enabled	RW	0
1	AGC1LEN	AGC1 Left channel Enabled 0: disabled 1: enabled	RW	0

0	AGC1REN	AGC1 Right channel Enabled 0: disabled 1: enabled	RW	0

11. Power Supply & Management Subsystem

11.1 Features

ATC260X PMU is a highly intergrated power management system. It supplies a solution for how to face the single chip lithium battery and the full power source which needs multipath power conversion output applications.

ATC260X PMU integrates 4 DCDC、12 LDO、2 load switch、10bit multiplex ADC、one linear charger、self-adaption power distribution control unit etc, automatic monitoring power's overvoltage, overcurrent, low-voltage, overtempreture etc abnormal conditions.

DCDC1 work in BUCK mode，input voltage range from 3.0v to 5.5v，and the **output voltage range from** 0.7v to 1.4v，the output voltage is adjustable with step of 25mv by setting the register，the current limit is 1.2A..
DCDC2 work in BUCK mode，input voltage range from 3.0v to 5.5v，and the **output voltage range from** 1.3 to 2.2v，the output voltage is adjustable with step of 50mv by setting the register ，the current limit is 1A.
DCDC3 work in BUCK mode，input voltage range from 3.0v to 5.5v，and the **output voltage range from** 2.6 to 3.3v，the output voltage is adjustable with step of 100mv by setting the register ，the current limit is 1A.
DCDC4 work in BOOST mode with external MOST,input voltage range from 3.0v to 5.5v，and the **output voltage is** 5v，the current limit is 800mA。
LDO1 input is SYSPWR，the output range is 2.6~3.3v adjusted，100mv per step，and the current limit is 400mA。
LDO2 input is SYSPWR，the output range is 2.6~3.3v adjusted, 100mv per step，and the current limit is 200mA。
LDO3 input is SYSPWR or DC3OUT，the output range is 1.5-2.0V adjusted,100mv per step，and the current limit is 250mA。
LDO4 input isSYSPWR，the output range is 2.8~3.5v adjusted，100mv per step，and the current limit is 400mA。
LDO5 input is SYSPWR，the output range is 2.6~3.3v adjusted，100mv per step，and the current limit is150mA。
LDO6 input is SYSPWR or DC3OUT，the output range is 0.7~1.4v adjusted，25mv per step，and the current limit is 200mA。
LDO7 input isSYSPWR orDC3OUT，the output range is 1.5~2.0v adjusted，100mv per step，the current limit is 200mA。

LDO8 input isSYSPWR，the output range is 2.3~3.3v adjusted，each rank is 100mv，the current limit is 150mA。
LDO9 input isSYSPWR orDC3OUT，the output range is 1.0~1.5v adjusted，100mv per step，the current limit is 150mA。
LDO10，the output range is 2.3~3.3v adjusted，100mv per step，the current limit is 100mA。
LDO11，input is SYSPWR，the output range is 2.6~3.3v adjusted，100mv per step，the current limit is 15mA，used for IO power of ATC260X
LDO12，the output range is 1.5~2.0v，used for RTC. in Standby mode.
There are two SWITCHS，it can configure as LDO mode or SWITCH mode. One current limit is 400mA，and the other is 100mA。
One linear charge-management for Li-Ion battery, the max charge current is 1.5A，it can adjust charging current automatically according to the current loading, includes trickle charge、CC、CV charging function, and it also has overcharge protection、timing protection and etc.
Support backup battery charging.
Self-adaption power distribution control module, self-adaption control the power distribution, power seamless handover of BAT、VBUS and WALL to ensure stable power supply.
The minimum Standby current is lower than 25uA
Overcurrent and overvoltage protection function of each power, and overtempreture protection of IC.
AuxADC，10-bit, 16-channel analog-to-digital converters (ADCs)，input voltage range is 0-3v，most circuit is used for monitoring the voltage, current and tempreture.

11.2 Module Description

11.2.1 Block Diagram

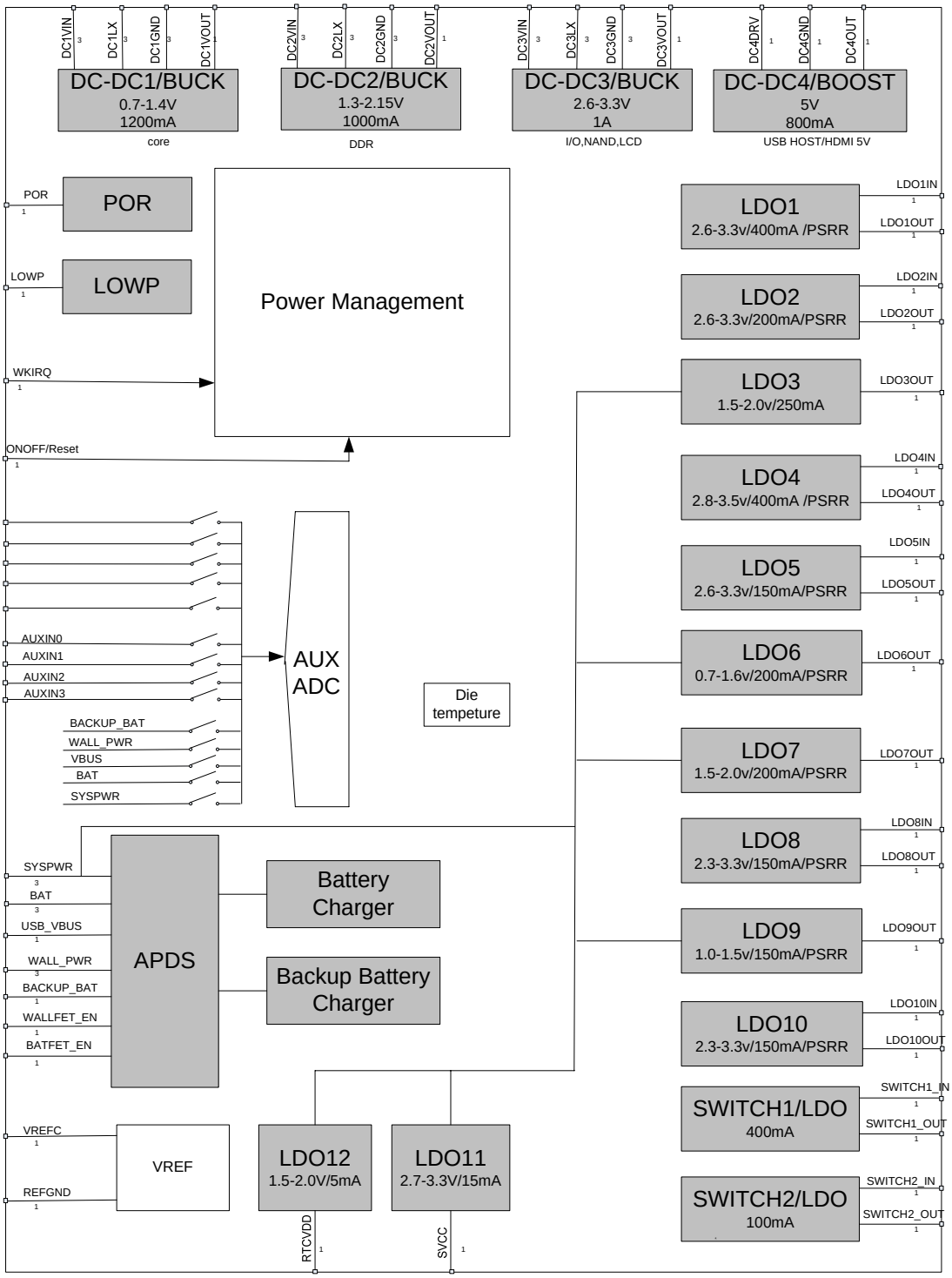


Figure 0-1

11.2.2 DCDC Module

ATC260x has four DCDC。

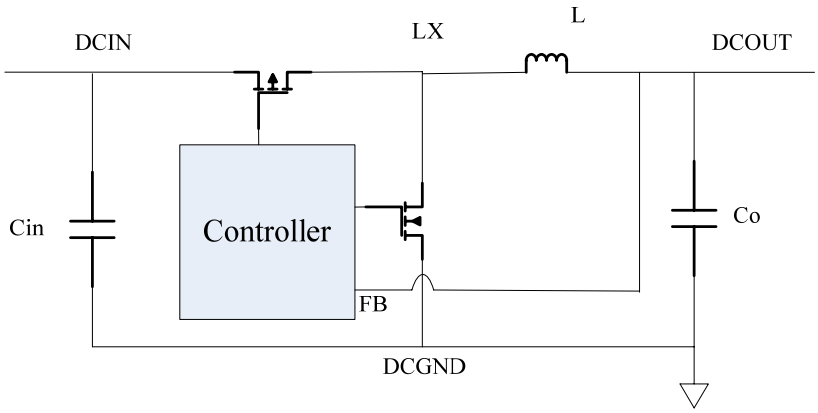


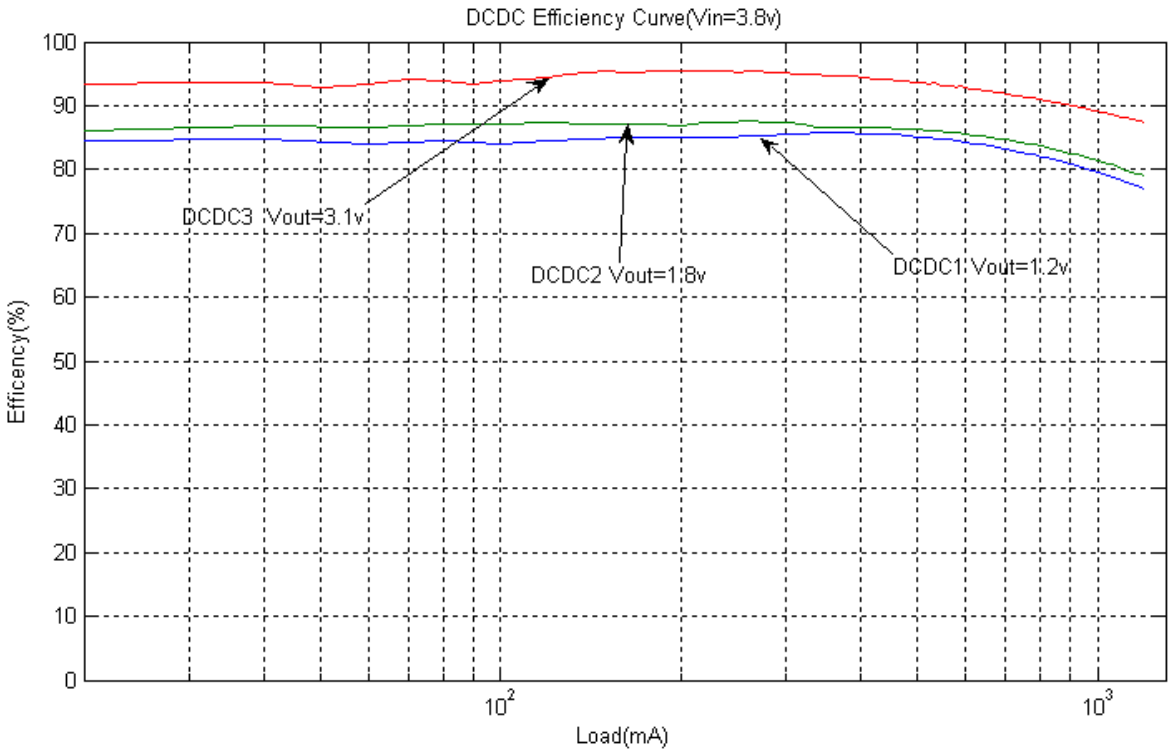
Figure 0-2 ATC260x BUCK DCDC circuit diagram

Three of these are BUCK DCDC，DCDC1，generates 0.7~1.4V voltage to supply the master core's need;DCDC2 generates 1.3~2.15v to supply the DDR's need;DCDC3 generates 2.6~3.3v to supply the power for master control and ATC260x's IO.

All of three BUCK DCDC integrate MOSFET inside, all of them are synchronization control, it can work normally only if installed one inductance and two capacitances outside.

Cin is a 10uF ceramic capacitor, and L is 2.2uH inductance, DCR<0.1Ohm，Co=10uF ceramic capacitor。

Buck DCDC efficiency curve is as follows：



The other is asynchronous boost DCDC, it mainly supplies power for USB OTG and HDMI,the maximum load capacity is 800mA, switch tube and FWD is external.

DCDC4 peripheral connection as follows:

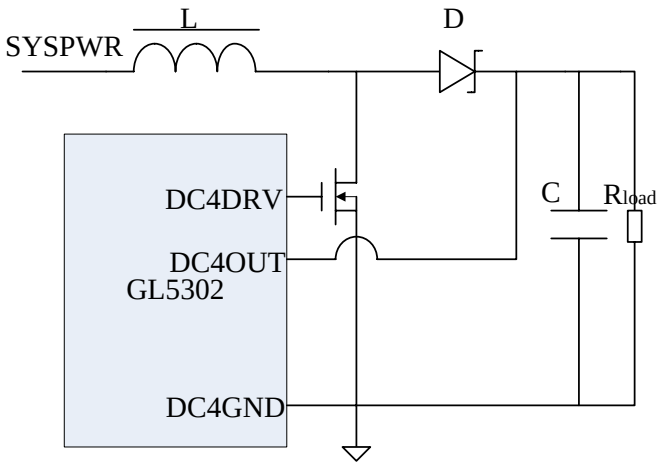


Figure 0-3

11.2.3 LDO Module

ATC260x has 12 LDO totally. the specifications as follows:

	input voltage(v)	output voltage(v)	max current(mA)	input capacitance/output capacitance	reference use
LDO1	3~5.5	2.6~3.3	400	0.1uF/2.2uF	master control AVCC
LDO2	3~5.5	2.6~3.3	200	0.1uF/2.2uF	ATC260xaudio+Ethernet
LDO3	3~5.5	1.5~2.0	250	0.1uF/2.2uF	ATC260x digital/sensor
LDO4	3~5.5	2.8~3.5	400	0.1uF/2.2uF	Wifi+bluetooth
LDO5	3~5.5	2.6~3.3	150	0.1uF/2.2uF	Sensor2.8v
LDO6	3~5.5	0.7~1.4	200	0.1uF/2.2uF	SATA+MIPI
LDO7	3~5.5	1.5~2.0	200	0.1uF/2.2uF	WIFI1.8
LDO8	3~5.5	2.3~3.3	150	0.1uF/2.2uF	FM+GPS
LDO9	3~5.5	1.0~1.5	150	0.1uF/2.2uF	WIFI1.2
LDO10	3~5.5	2.3~3.3	100	0.1uF/2.2uF	SATA2.5
LDO11	3-5.5	2.6~3.3	15	0.1uF/1.0uF	SVCC
LDO12	3-5.5	1.5~2.0	5	0.1uF/1.0uF	RTCVDD

LDO has output overvoltage protection, output overcurrent protection and output low-voltage function.

When the LDO output voltage beyond the overvoltage protection range, LDO will overvoltage suspend,and whether LDO overvoltage enabled,it all depends on register.

When LDO output voltage lower than low-voltage protection, LDO low-protection suspend will be sent out, and whether LDO low-voltage enabled, it all depends on register.

11.2.4 SWITCH Module

ATC260x has two switches. SWITCH1 is used in generating the SD card power, its input is DC3OUT,the current limit is 400mA.

And,SWITCH1 can be config as LDO. When choose LDO mode, LDO output 3.0~3.3v, in that mode, its input usually chooses SYSPWR.

SWITCH2 input is DC3OUT， its current limit is 100mA。

SWITCH2 can also be config as LDO, when choose LDO mode, LDO output 1.0~3.3v,in that mode , its input usually selects SYSPWR.

11.2.5 CHARGER Module

ATC260X integrates a constant current/constant voltage charger. It can adjust the charging current by power dissipation. It also has battery detecting and trickle charging function.

When insert a external adaptor,and detecting the SYSPWR voltage is higher than BAT,the charger will enabled by software and the ATC260X PMU can config charging process automatically.

ATC260X PMU dectects whether the battery is exist or not depend on the BAT PIN voltage.

Charge current can set by register, the max current is 1.5A. the reality charging current can read by charging current ADC register.

In process of charging,the IC inner tempreture and battery tempreture is monitored all the time, if the tempreture is higher or lower than the standard value,suspend signal will send, software is going to take measures and charging paused.

Measuring battery’s tempreture by Temp PIN.

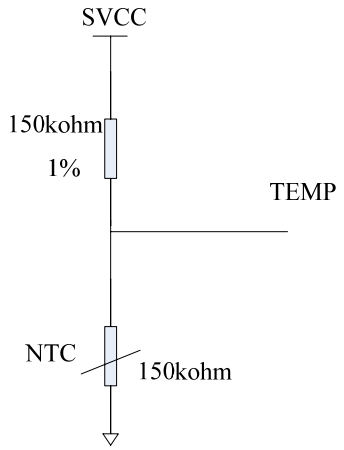


Figure 0-4 ATC260x battery tempreture detecting diagram

ATC260X supports backup battery charging, when the master battery powered down,backup battery can supply RTC power and save the time and other information of system. You can choose Li-Ion battery or 3v button battery as backup battery and the charging current can be set.

11.2.6 APDS Module

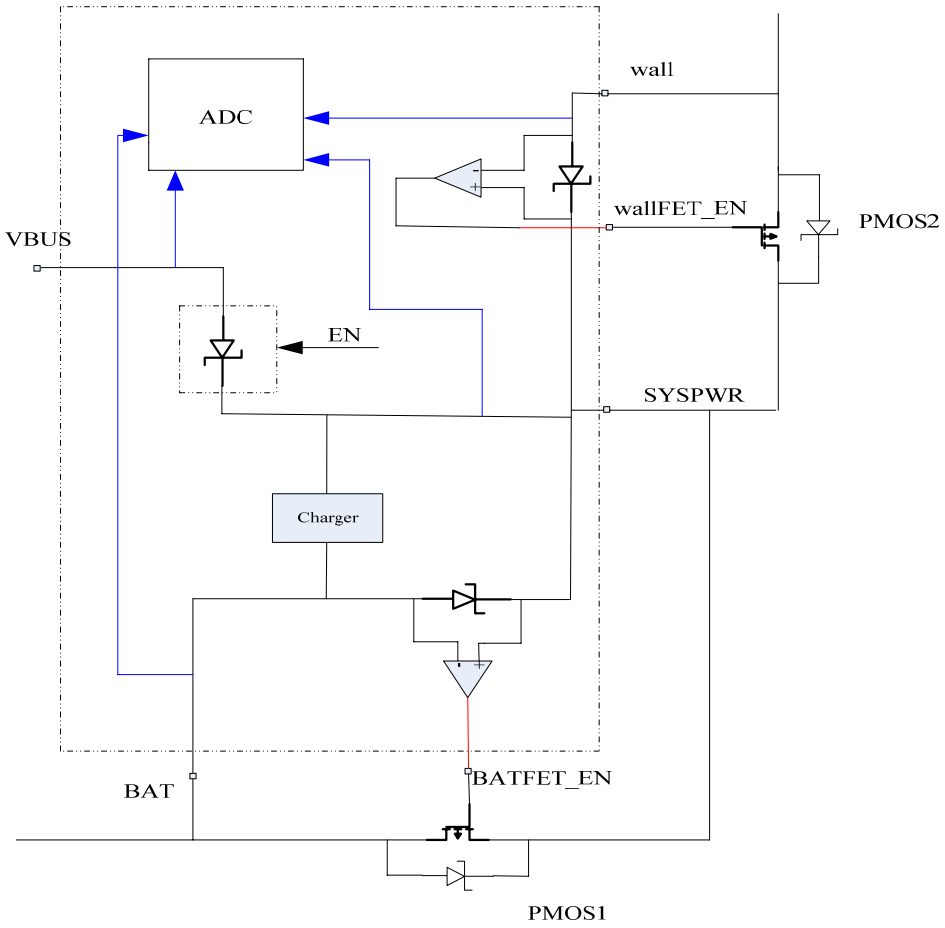


Figure 0-5

ATC260x APDS（Adaptive Power Distribute System）block diagram as shown above. ATC260x PMU get power from BAT、VBUS and WALL.SYSPWR is a public taking power node, both DCDC and LDO take power from this node. VBUS connects to SYSPWR through IC internal ideal diode(ID). In order to avoide VBUS current flowing to SYSPWR in OTG application, The ID from VBUS to SUSPWR has an enabled control.When the ID is disable, VBUS and SYSPWR will be cut off completely.

ATC260xPMU needs to provide large power, in order to reduce circuit heat loss,two external MOS is necessery, Which as the block diagram show PMOS1 and PMOS2. In IC Between BAT and SYSPWR,there is a ideal diode, the same as WALL and SYSPWR.

ATC260x can detect BAT、VBUS、WALL and SYSPWR voltage at the same time. It also can detect current which flows to ideal diode.

When BAT output voltage beyond setting, it will send BAT overvoltage suspend. When BAT voltage lower than setting, it will send BAT low-voltage suspend. When BAT current beyond setting, it will send BAT overcurrent suspend; When BAT current beyond overcurrent shut-off setting, the power will be force to shut off to protect IC.

When VBUS voltage higher than settings, it will send VBUS overvoltage suspend. When VBUS

voltage lower than settings, it will send VBUS low-voltage suspend. When VBUS current beyond setting, it will send VBUS overcurrent suspend. When VBUS current beyond overcurrent shut-off setting, it also will force to shut off power to protect IC.

When WALL voltage higher than setting, it will send WALL overvoltage suspend. When WALL voltage lower than setting, it will send WALL low-voltage suspend. When WALL current beyond setting, it will send WALL overcurrent suspend. When WALL current beyond overcurrent shut-off setting, it will also force to shut off power to protect IC.

When SYSPWR voltage higher than setting, it will send SYSPWR overvoltage suspend.

11.2.7 Standby Module

According to the application, the power states is divided as follows:

S1- Working Mode：

In S1， master can work normally, and its kernel and IO can also operate normally, that is to say, both DCDC1 and DCDC3 work regularly and communicate with ATC260X normally. LDO6 and LDO1 needed by the corresponding master should be work normally. This state called S1.

S2- Standby Mode：

When both master IC’s kernel and IO shut off, its essential information saves in DDR so that start fast. At this time, DCDC2 work normally, master and ATC260x can not communicate. We called this state S2.

S3-Sleep Mode：

When we don’t use it in a long time, DDR apparatus also can shut off to enter S3 state.

S4- Deep Sleep Mode：

When Standby power dissipation is minimum, entering S4 state.

Wakeup elements:

ATC260x has the following wakeup elements:

ONOFF button、Alarm、TP、WKIRQ、Reset、Rem_con、VBUS、Wall、HDSW、IR。

In S2，all wakeup elements can wake up.

In S3，all wakeup elements can wake up.

In S4，only exist RTCVDD，SVCC shut off，so WKIRQ、TP、Rem_con、IR can not wake up，the other wakeup elements can wake up.

Either long or short press ONOFF button can wake up,it all depends on register.

In S1，software can configurate into S2、S3 or S4 by setting the EN_S1、EN_S2、EN_S3 bits as follow.

power state	EN_S1	EN_S2	EN_S3
S4	0	0	0
S3	0	0	1
S2	0	1	x
S1	1	x	x

When in S1 mode, it is need to enter S2, we can configure EN S2=1 first, then write 0 to EN_S1, it will enter S2 state.

Overcurrent protection

If LDO1、LDO2、LDO3 or LDO6 is overcurrent, then pull down PWROK, and entering standby state according to EN_S2, EN_S3.

If BAT、WALL or VBUS overcurrent, and it is enabled to its corresponding overcurrent shutoff, then entering Standby state according to EN_S2 and EN_S3。

Overtempreture protection

When IC is overtempreture, and the overtempreture protect is enabled, then entering Standby state by EN_S2 and EN_S3.

11.2.8 POR and power on/off sequence Module

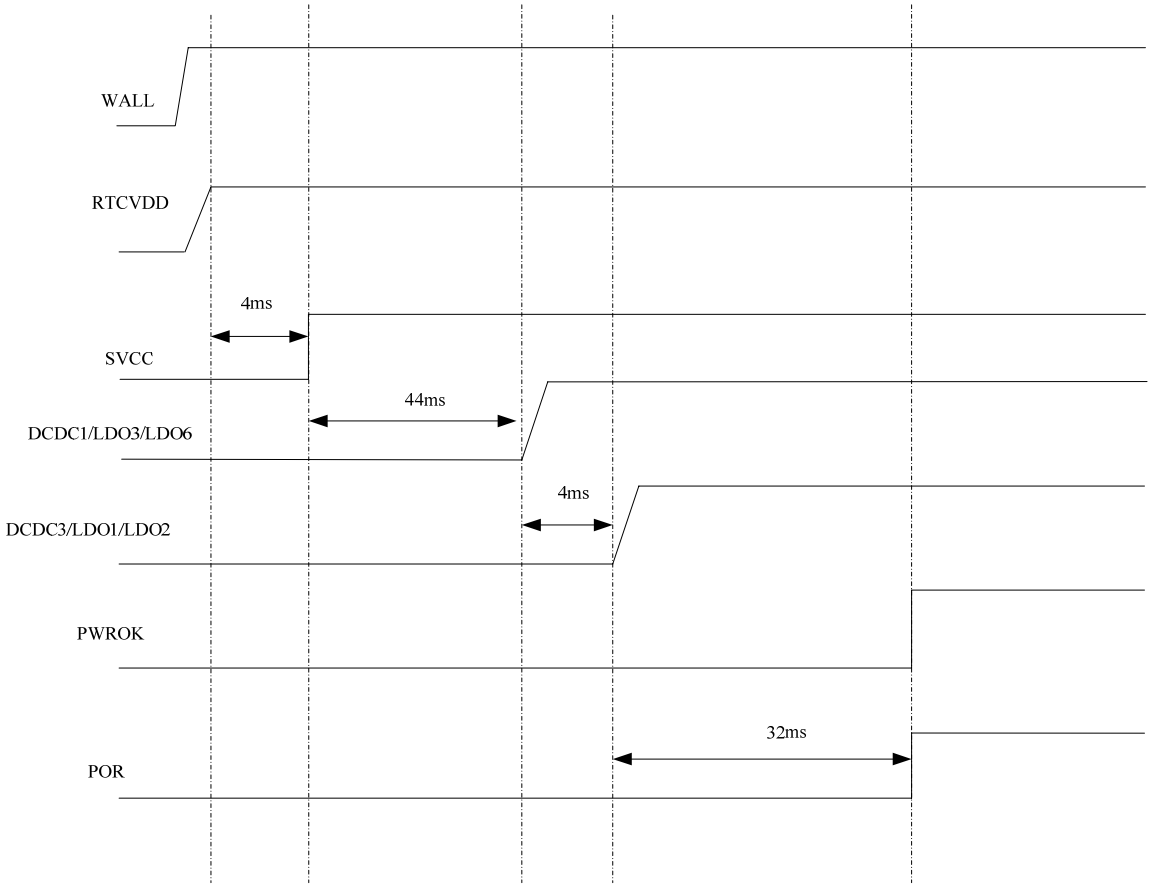


Figure 0-6 power on sequence

ATC260x power on process is to turn on the power of BAT or WALL or VBUS, then generating RTCVDD and SVCC. After that, ATC260x's 1.8v kernel voltage and master's kernel 1.0v voltage will be produced. Then generating ATC260x and master's high-voltage part. At last, when all the power is stable, sending POR to master, it can start to run.

If it is software powered down, master sends order to ATC260x, and ATC260x receiving the order to pull down the PWROK and POR, then shut off DCDC1、DCDC3、LDO1、LDO2、LDO3 and LDO6。

If it is force to power down, the ATC260x will pull down PWROK and POR when it detects any of signals of DC1OUTOK、DC3OUTOK、LDO1OUTOK、LDO2OUTOK、LDO3OUTOK and LDO6OUTOK is pulled down.

11.2.9 ONOFF&Reset Module

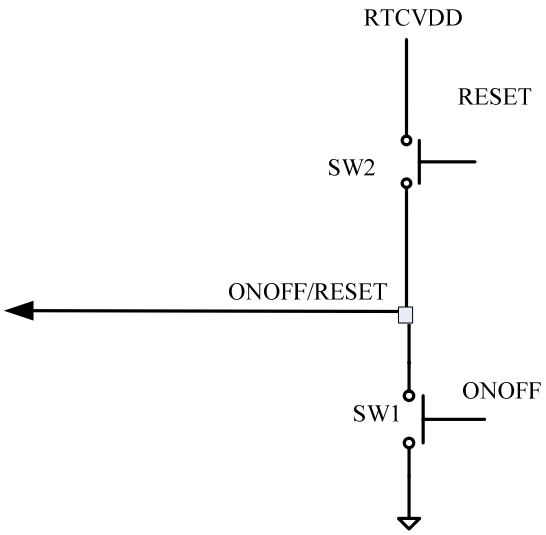


Figure 0-7

In the ATC260x PMU,ONOFF and Reset multiplex the same PIN, as shown above. The SYSRST or SYSONOFF signal will be generated by the voltage at the PIN, it is sent to handle by corresponding circuit. If pressing Reset and ONOFF button at the same time, it will reset all registers in RTCVDD voltage region.

When long press ONOFF button beyond the setting time 6s、8s、10s、12s, it will send the same signal as P_Reset to reset the whole system.

11.3 Register List

PMU Block Address

Name	Base Address
PMU	0x0000

Table 0-1 **PMU Controller Registers**

Offset	Register Name	Description
0x00	PMU_SYS_CTL0	PMU SYSTEM CONTROL Register0
0x01	PMU_SYS_CTL1	PMU SYSTEM CONTROL Register1
0x02	PMU_SYS_CTL2	PMU SYSTEM CONTROL Register2
0x03	PMU_SYS_CTL3	PMU SYSTEM CONTROL Register3
0x04	PMU_SYS_CTL4	PMU SYSTEM CONTROL Register4

0x05	PMU_SYS_CTL5	PMU SYSTEM CONTROL Register5
0x06	PMU_SYS_CTL6	PMU SYSTEM CONTROL Register6
0x07	PMU_SYS_CTL7	PMU SYSTEM CONTROL Register7
0x08	PMU_SYS_CTL8	PMU SYSTEM CONTROL Register8
0x09	PMU_SYS_CTL9	PMU SYSTEM CONTROL Register9
0x0A	PMU_BAT_CTL0	PMU BAT CONTROL Register0
0x0B	PMU_BAT_CTL1	PMU BAT CONTROL Register1
0x0C	PMU_VBUS_CTL0	PMU VBUS CONTROL Register0
0x0D	PMU_VBUS_CTL1	PMU VBUS CONTROL Register1
0x0E	PMU_WALL_CTL0	PMU WALL CONTROL Register0
0x0F	PMU_WALL_CTL1	PMU WALL CONTROL Register1
0x10	PMU_SYS_Pending	PMU SYSTEM Pending Register
0x11	PMU_DC1_CTL0	PMU DCDC1 CONTROL Register0
0x12	PMU_DC1_CTL1	PMU DCDC1 CONTROL Register1
0x13	PMU_DC1_CTL2	PMU DCDC1 CONTROL Register2
0x14	PMU_DC2_CTL0	PMU DCDC2 CONTROL Register0
0x15	PMU_DC2_CTL1	PMU DCDC2 CONTROL Register1
0x16	PMU_DC2_CTL2	PMU DCDC2 CONTROL Register2
0x17	PMU_DC3_CTL0	PMU DCDC3 CONTROL Register0
0x18	PMU_DC3_CTL1	PMU DCDC3 CONTROL Register1
0x19	PMU_DC3_CTL2	PMU DCDC3 CONTROL Register2
0x1A	PMU_DC4_CTL0	PMU DCDC4 CONTROL Register0
0x1B	PMU_DC4_CTL1	PMU DCDC4 CONTROL Register1
0x1E	PMU_LDO1_CTL	PMU LDO1 CONTROL Register
0x1F	PMU_LDO2_CTL	PMU LDO2 CONTROL Register
0x20	PMU_LDO3_CTL	PMU LDO3 CONTROL Register
0x21	PMU_LDO4_CTL	PMU LDO4 CONTROL Register
0x22	PMU_LDO5_CTL	PMU LDO5 CONTROL Register
0x23	PMU_LDO6_CTL	PMU LDO6 CONTROL Register
0x24	PMU_LDO7_CTL	PMU LDO7 CONTROL Register
0x25	PMU_LDO8_CTL	PMU LDO8 CONTROL Register
0x26	PMU_LDO9_CTL	PMU LDO9 CONTROL Register
0x27	PMU_LDO10_CTL	PMU LDO10 CONTROL Register
0x28	PMU_LDO11_CTL	PMU LDO11 CONTROL Register
0x29	PMU_SWITCH_CTL	PMU SWITCH CONTROL Register
0x2A	PMU_OV_CTL0	PMU OVER VOLTAGE CONTROL Register0

0x2B	PMU_OV_CTL1	PMU OVER VOLTAGE CONTROL Register1
0x2C	PMU_OV_Status	PMU OVER VOLTAGE Status Register
0x2D	PMU_OV_EN	PMU OVER VOLTAGE Detect ENABLE Register
0x2E	PMU_OV_INT_EN	PMU OVER VOLTAGE INT ENABLE Register
0x2F	PMU_OC_CTL	PMU OVER CURRENT CONTROL Register
0x30	PMU_OC_Status	PMU OVER CURRENT Status Register
0x31	PMU_OC_EN	PMU OVER CURRENT Detect ENABLE Register
0x32	PMU_OC_INT_EN	PMU OVER CURRENT INT ENABLE Register
0x33	PMU_UV_CTL0	PMU UNDER VOLTAGE CONTROL Register0
0x34	PMU_UV_CTL1	PMU UNDER VOLTAGE CONTROL Register1
0x35	PMU_UV_Status	PMU UNDER VOLTAGE Status Register
0x36	PMU_UV_EN	PMU UNDER VOLTAGE Detect ENABLE Register
0x37	PMU_UV_INT_EN	PMU UNDER VOLTAGE INT ENABLE Register
0x38	PMU_OT_CTL	PMU OVER TEMPERTURE CONTROL Register
0x39	PMU_CHARGER_CTL0	PMU CHARGER CONTROL Register0
0x3A	PMU_CHARGER_CTL1	PMU CHARGER CONTROL Register1
0x3B	PMU_CHARGER_CTL2	PMU CHARGER CONTROL Register2
0x3C	PMU_BakCHARGER_CTL	PMU BakCHARGER CONTROL Register
0x3D	PMU_APDS_CTL	PMU APDS CONTROL Register

11.4 Register Description

11.4.1 PMU_SYS_CTL0

PMU_SYS_CTL0 Register（default 0xe055）
Offset = 0x00

Bit(s)	Name	Description	R/W	Reset
15	USB_WK_EN	VBUS wake up enable 1：VBUS beyond the setting voltage can wake up 0：VBUS beyond the setting voltage cannot wake up	R/W	0x1
14	WALL_WK_EN	WALL wake up enable 1：WALL beyond the setting voltage can wake up	R/W	0x1

		0：WALL beyond the setting voltage cannot wake up		
13	ONOFF_LONG_WK_EN	ONOFF long press to wake up enable 1：ONOFF long press can wake up 0：ONOFF long press cannot wake up	R/W	0x1
12	ONOFF_SHORT_WK_EN	ONOFF short press wake up enable 1：ONOFF short press can wake up 0：ONOFF short press cannot wake up	R/W	0x0
11	WKIRQ_WK_EN	WKIRQ wake up enable 1：WKIRQ can wake up 0：WKIRQ cannot wake up	R/W	0x0
10	TP_WK_EN	TP wake up enable 1：TP touch can wake up 0：TP touch cannot wake up	R/W	0x0
9	Rem_con_WK_EN	Rem_con wake up enable 1：Rem_con button can wake up 0：Rem_con button cannot wake up	R/W	0x0
8	Alarm_WK_EN	Alarm wake up enable 1：Alarm can wake up 0：Alarm cannot wake up	R/W	0x0
7	HDSW_WK_EN	Hard switching wake enable 0：No 1：Yes	R/W	0x0
6	Reset_WK_EN	Reset wake up enable 0：No 1：Yes	R/W	0x1
5	IR_WK_EN	IR wake up enable 0：No 1：Yes	R/W	0x0
4:3	VBUS_WK_TH	VBUS wake up threshold 00：4.05V 01：4.2V 10：4.35V 11：4.5V	R/W	10
2:1	WALL_WK_TH	WALL wake up threshold 00：4.05V 01：4.2V 10：4.35V 11：4.5V	R/W	10
0	ONOFF_MUXKEY_EN	ONOFF multiplex button enable	R/W	0x1

		0：Disable（No Preset button） 1：Enable （Have Preset button）		

11.4.2 PMU_SYS_CTL1

PMU_SYS_CTL1 Register （default 0x000e）
Offset = 0x01

Bit(s)	Name	Description	R/W	Reset
15	USB_WK_Flag	VBUS wake up Flag 1：Vbus wake up happened 0：NO VBUS wake up	R	0x0
14	WALL_WK_ Flag	WALL wake up Flag 1：WALL wake up happen 0：No WALL wake up	R	0x0
13	ONOFF_LONG_WK_ Flag	ONOFF long press button wake up Flag 1：long press ONOFF button to wake up happened 0：Not long press ONOFF button to wake up	R	0x0
12	ONOFF_SHORT_WK_ Flag	ONOFF press button to wake up 1：long press ONOFF to wake up happened 0：no long press ONOFF to wake up	R	0x0
11	WKIRQ_WK_ Flag	WKIRQ wake up Flag 1：WKIRQ wake up happened 0：not WKIRQ to wake up	R	0x0
10	TP_WK_ Flag	TP wake up Flag 1：TP wake up happened 0：not TP to wake up	R	0x0
9	Rem_con_WK_ Flag	Rem_con wake up Flag 1：Rem_con to wake up happened 0：not Rem_con to wake up	R	0x0
8	Alarm_WK_ Flag	Alarm wake up Flag 1：Alarm to wake up happened 0：not Alarm to wake up	R	0x0
7	HDSW_WK_ Flag	HDSW wake up Flag 1：HDSW to wake up happened 0：not HDSW to wake up	R	0x0
6	RESET_WK_ Flag	Reset wake up Flag	R	0x0

		1：reset to wake up happened 0：not reset to wake up		
5	IR_WK_ Flag	IR wake Flag 1：IR to wake up happened 0：not IR to wake up	R	0x0
4:3	LB_S4	Low power to enter S4 voltage setting 00：2.9V 01：3.0V 10：3.1V 11：3.3V System is in S1、S2、S3，when BAT voltage lower than the settings, and there's no USB and WALL, entering S4 mode directly	R/W	01
2	LB_S4_EN	Low power entering S4 enable(it contains detecting enable) 0：Disable 1：Enable	R/W	0x1
1	ENRTCOSC	internal 32k clock enable 0：disable 1：enable	R/W	0x1
0	EN_S1	entering S1 state enable 0：no entering S1 1：entering S1	R/W	0x0

11.4.3 PMU_SYS_CTL2

PMU_SYS_CTL2 Register （default 0x0680）
Offset = 0x02

Bit(s)	Name	Description	R/W	Reset
15	ONOFF_PRESS	Whether ONOFF button is pressed 0：ONOFF is not pressed 1：ONOFF is pressed	R	0x0
14	ONOFF_SHORT_PRESS	ONOFF short press pending 0: no short press ONOFF button 1: short press ONOFF button Write 1 clear 0	R/W	0x0
13	ONOFF_LONG_PRESS	ONOFF long press pending 0: no long press ONOFF button	R/W	0x0

		1: long press ONOFF button Write 1 clear 0		
12	ONOFF_INT_EN	ONOFF suspend enbale 0：disable 1：enable	R/W	0x0
11:10	ONOFF_PRESS_TIME	ONOFF setting by time of press button： 00: 60ms < t < 0.5s, judged as short press; t >=0.5s, judged as long press; 01: 60ms < t < 1s, judged as short press; t >=1s, judged as long press; 10: 60ms < t < 2s, judged as short press; t >=2s, judged as long press; 11: 60ms < t < 4s, judged as short press; t >=4s, judged as long press;	R/W	01
9	ONOFF_Reset_EN	ONOFF long press reset function enable 0：disable 1：enable	R/W	1
8：7	ONOFF_Reset_Time_SEL	long press ONOFF and send Reset time selection 00：6s 01：8s 10：10s 11：12s	R/W	01
6	S2_timer_EN	S2_timer_EN 0:Disable 1:Eanbel When S2timer enabled，entering S2，S2timer starts to time, when time to the settings, entering S3	R/W	0x0
5：3	S2timer	S2timer 000：6min 001：16min 010：31min 011：61min 100：91min 101：121min 110：151min 111：181min	R/W	0x0

2:0	Reserved	Reserved	R/W	0x0

11.4.4 PMU_SYS_CTL3

PMU_SYS_CTL3 Register （default 0x0000）
Offset = 0x03

Bit(s)	Name	Description	R/W	Reset
15	EN_S2	Entering S2 state enable 0：no entering S2 1：entering S2	R/W	0x0
14	EN_S3	Entering S3 state enbale 0：no entering S3 1：entering S3	R/W	0x0
13	S3_timer_EN	S3_timer_EN 0:Disable 1:Eanbel When S3timer enabled, enting S3，S3timer starts to time, when time to the settings, entering S4	R/W	0x0
12：10	S3timer	S3timer 000：6min 001：16min 010：31min 011：61min 100：91min 101：121min 110：151min 111：181min	R/W	0x0
9：4	Reserved	Reserved	R/W	0x0
3	IR_PIN_TYPE	Configure IR PIN for different functions 0：IR 1：GPIO	R/W	0
2	IR _GPIO_Output_en	Configure IR PIN’s GPIO to output enable 0：Disable 1：Enable	R/W	0

1	IR _GPIO_Intput_en	Configure IR's GPIO to input enable 0：Disable 1：Enable	R/W	0
0	IR_GPIO_DATA	IR's GPIO DATA	R/W	0

11.4.5 PMU_SYS_CTL4

PMU_SYS_CTL4 Register （default 0x0080）

Offset = 0x04

Bit(s)	Name	Description	R/W	Reset
15	WKIRQ_PIN_TYPE	Configure WKIRQ PIN for different functions 0：WKIRQ 1：GPIO	R/W	0
14	WKIRQ_GPIO_Output_en	Configure WKIRQ's GPIO output enable 0：Disable 1：Enable	R/W	0
13	WKIRQ_GPIO_Intput_en	configure WKIRQ's GPIO to output enable 0：Disable 1：Enable	R/W	0
12	WKIRQ_GPIO_DATA	WKIRQ's GPIO DATA	R/W	0
11：10	WKIRQ_TPYE	WKIRQ's type 00：High level active 01：Low level active 10：Rising edge- triggered 11：Falling edge-triggered	R/W	00
9	WKIRQ_32K_EN	Configure WKIRQ PIN to send out 32K clock 0：WKIRQ's function is defined by bit15 1：WKIRQ send out 32K clock	R/W	0x0
8	Reserved	Reserved	R/W	0x0
7	LOWP _GPIO_Output_en	Configure LOWP's GPIO to output enable 0：Disable 1：Enable	R/W	1
6	LOWP _GPIO_Intput_en	Configure LOWP's GPIO to input	R/W	0

		enable 0：Disable 1：Enable		
5	LOWP _GPIO_DATA	LOWP 的 GPIO DATA	R/W	0
4	LOWP_32K_EN	Configure LOWP PIN to send out 32K clock 0：LOWP make GPIO 1：LOWP send out 32K clock	R/W	0x0
3：2	Reserved	Reserved	R/W	0x0
1	WKIRQ_EN	WKIRQ interrupt enable 0: disable 1: enable	R/W	0
0	WKIRQ_PD	WKIRQ pending 0：WKIRQ is not active 1：WKIRQ is active Write 1 clear 0	R/W	0

11.4.6 PMU_SYS_CTL5

PMU_SYS_CTL5 Register （default 0x0180）

Offset = 0x05

Bit(s)	Name	Description	R/W	Reset
15：1	Reserved	Reserved	R/W	0x0
10	TP_DECT_EN	TP wake up detecting enable 0: Disable 1:Enable	R/W	0
9	REMCON_DECT_EN	Remcon wake up detecting enable 0: Disable 1:Enable	R/W	0
8	VBUSWKDTEN	VBUS wakeup detect enable 0: Disable 1:Enable	R/W	1
7	WALLWKDTEN	WALL wakeup detect enable 0: Disable 1:Enable	R/W	1
6 ： 0	Reserved	Reserved	R/W	0

11.4.7 PMU_SYS_CTL6

PMU_SYS_CTL6 Register （default 0x0000）
Offset = 0x06

Bit(s)	Name	Description	R/W	Reset
15：0	Reserved	Reserved	R/W	0x0

11.4.8 PMU_SYS_CTL7

PMU_SYS_CTL7 Register （default 0x0000）
Offset = 0x07

Bit(s)	Name	Description	R/W	Reset
15：0	Reserved	Reserved	R/W	0x0

11.4.9 PMU_SYS_CTL8

PMU_SYS_CTL8 Register （default 0x0000）
Offset = 0x08

Bit(s)	Name	Description	R/W	Reset
15：0	Reserved	No reset by Preset and ONOFFRESET	R/W	0x0

11.4.10PMU_SYS_CTL9

PMU_SYS_CTL9 Register （default 0x0000）
Offset = 0x09

Bit(s)	Name	Description	R/W	Reset
15：0	Reserved	No reset by Preset and ONOFFRESET	R/W	0x0

11.4.11 PMU_BAT_CTL0

PMU_BAT_CTL0 Register （default 0x5680）
Offset = 0x0A

Bit(s)	Name	Description	R/W	Reset
15：14	BAT_UV_VOL	BAT undervoltage suspend voltage setting 00：3.1V 01：3.3V 10：3.4V 11：3.5V	R/W	01
13:12	BAT_OV_VOL	BAT overvoltage suspend voltage setting 00：4.3V 01：4.4V 10：4.5V 11：4.8V	R/W	01
11:8	BAT_OC_Set	BAT overcurrent suspend current setting 0000：200mA 0001：250mA 0010：300mA 0011：350mA 0100：400mA 0101：450mA 0110：500mA 0111：550mA 1000：600mA 1001：650mA 1010：700mA 1011：750mA 1100：800mA 1101：850mA 1110：900mA 1111：950mA The detecting current is flowing from BAT to SYSPWR ideal diode Overcurrent signal Debounce 1ms	R/W	0110
7：6	BAT_OC_ SHUTOFF _Set	BAT ouvercurrent shutoff current setting 00：600mA 01：800mA 10：1000mA 11：1200mA Overcurrent signal Debounce 1ms	R/W	10
5：0	Reserved	Reserved	R/W	0x0

11.4.12 PMU_BAT_CTL1

PMU_BAT_CTL1 Register （default 0xfc00）
Offset = 0x0B

Bit(s)	Name	Description	R/W	Reset
15	BAT_OC_EN	BAT overcurrent detect enable 0：disable 1：enable	R/W	1
14	BAT_OV_EN	BAT overvoltage detect enable 0：disable 1：enable	R/W	1
13	BAT_UV_EN	BAT undervoltage detect enable 0：disable 1：enable	R/W	1
12	BAT_OC_INT_EN	BAT overcurrent suspend enable 0：disable 1：enable	R/W	1
11	BAT_OV_INT _EN	BAT overvoltage suspend enable 0：disable 1：enable	R/W	1
10	BAT_UV_INT _EN	BAT undervoltage suspend enable 0：disable 1：enable	R/W	1
9	BAT_OC_SHUTOFF_EN	BAT overcurrent shutoff enable 0：disable 1：enable	R/W	0
8：0	Reserved	Reserved	R/W	0x0

11.4.13 PMU_VBUS_CTL0

PMU_VBUS_CTL0 Register （default 0xa680）
Offset = 0x0C

Bit(s)	Name	Description	R/W	Reset
15：14	VBUS_UV_VOL	VBUS undervoltage suspend voltage setting 00：3.8V	R/W	10

		01：4.0V 10：4.3V 11：4.5V		
13:12	VBUS_OV_VOL	VBUS overvoltage suspend voltage setting 00：5.3V 01：5.5V 10：5.6V 11：5.8V	R/W	10
11:8	VBUS_OC_Set	VBUS overcurrent suspend voltage setting 0000：100mA 0001：500mA 0010：600mA 0011：700mA 0100：800mA 0101：900mA 0110：1000mA Others：reserved The detecting current is flowing from BAT to SYSPWR ideal diode overcurrent signal Debounce 1ms	R/W	0110
7：6	VBUS_OC_ SHUTOFF _Set	VBUS overcurrent shutoff current setting 00：600mA 01：800mA 10：1000mA 11：1200mA overcurrent signal Debounce 1ms	R/W	10
5：0	Reserved	Reserved	R/W	0x0

11.4.14 PMU_VBUS_CTL1

PMU_VBUS_CTL1 Register （default 0xfc00）

Offset = 0x0D

Bit(s)	Name	Description	R/W	Reset
15	VBUS_OC_EN	VBUS overcurrent detecting enable 0：disable 1：enable	R/W	1

14	VBUS_OV_EN	VBUS overvoltage detecting enable 0：disable 1：enable	R/W	1
13	VBUS_UV_EN	VBUS undervoltage detecting enable 0：disable 1：enable	R/W	1
12	VBUS_OC_INT_EN	VBUS overcurrent suspend enable 0：disable 1：enable	R/W	1
11	VBUS_OV_INT _EN	VBUS overvoltage suspend enable 0：disable 1：enable	R/W	1
10	VBUS_UV_INT _EN	VBUS undervoltage suspend enable 0：disable 1：enable	R/W	1
9	VBUS_OC_SHUTOFF_EN	VBUS overcurrent shutoff enable 0：disable 1：enable	R/W	0
8：0	Reserved	Reserved	R/W	0x0

11.4.15 PMU_WALL_CTL0

PMU_WALL_CTL0 Register （default 0xE680）
Offset = 0x0E

Bit(s)	Name	Description	R/W	Reset
15：14	WALL_UV_VOL	WALL undervoltage suspend voltage setting 00：3.8V 01：4.0V 10：4.3V 11：4.5V	R/W	11
13:12	WALL_OV_VOL	WALL overvoltage suspend voltage setting 00：5.3V 01：5.5V 10：5.6V 11：5.8V	R/W	10
11:8	WALL_OC_Set	WALL overcurrent suspend current	R/W	0110

		setting 0000：200mA 0001：250mA 0010：300mA 0011：350mA 0100：400mA 0101：450mA 0110：500mA 0111：550mA 1000：600mA 1001：650mA 1010：700mA 1011：750mA 1100：800mA 1101：850mA 1110：900mA 1111：950mA The detecting current is flowing from BAT to SYSPWR ideal diode Overcurrent signal Debounce 1ms		
7：6	WALL_OC_ SHUTOFF _Set	WALL overcurrent shutoff current setting 00：600mA 01：800mA 10：1000mA 11：1200mA Overcurrent signal Debounce 1ms	R/W	10
5：0	Reserved	Reserved	R/W	0x0

11.4.16 PMU_WALL_CTL1

PMU_WALL_CTL1 Register （default 0xfc00）

Offset = 0x0F

Bit(s)	Name	Description	R/W	Reset
15	WALL_OC_EN	WALL overcurrent detect enable 0：disable 1：enable	R/W	1

14	WALL_OV_EN	WALL overvoltage detect enable 0：disable 1：enable	R/W	1
13	WALL_UV_EN	WALL undervoltage detect enable 0：disable 1：enable	R/W	1
12	WALL_OC_INT_EN	WALL overcurrent suspend enable 0：disable 1：enable	R/W	1
11	WALL_OV_INT _EN	WALL overvoltage suspend enable 0：disable 1：enable	R/W	1
10	WALL_UV_INT _EN	WALL undervoltage suspend enable 0：disable 1：enable	R/W	1
9	WALL_OC_SHUTOFF_EN	WALL overcurrent shutoff enable 0：disable 1：enable	R/W	0
8：0	Reserved	Reserved	R/W	0x0

11.4.17 PMU_SYS_Pending

PMU_SYS_Pending Register （default 0x0000）
Offset = 0x10

Bit(s)	Name	Description	R/W	Reset
15	BAT_OV_STATUS	BAT overvoltage state indication 0：present BAT votage is not overvoltage 1：present BAT voltage is overvotage	R	0x0
14	BAT_UV_STATUS	BAT undervoltage state indication 0：present BAT votage is not undervoltage 1：present BAT voltage is undervotage	R	0x0
13	BAT_OC_STATUS	BAT overcurrent state indication 0：present BAT current is not overcurrent	R	0x0

		1 ： present BAT current is overcurrent		
12	VBUS_OV_STATUS	VBUS overvoltage state indication 0 ： present BAT votage is not overvoltage 1 ： present BAT voltage is overvotage	R	0x0
11	VBUS _UV_STATUS	VBUS undervoltage state indication 0 ： present BAT votage is not undervoltage 1 ： present BAT voltage is undervotage	R	0x0
10	VBUS _OC_STATUS	VBUS overcurrent state indication 0 ： present BAT current is not overcurrent 1 ： present BAT current is overcurrent	R	0x0
9	WALL_OV_STATUS	WALL overvoltage state indication 0 ： present BAT votage is not overvoltage 1 ： present BAT voltage is overvotage	R	0x0
8	WALL _UV_STATUS	WALL undervoltage state indication 0 ： present BAT votage is not undervoltage 1 ： present BAT voltage is undervotage	R	0x0
7	WALL _OC_STATUS	WALL overcurrent state indication 0 ： present BAT current is not overcurrent 1 ： present BAT current is overcurrent	R	0x0
6：1	Reserved	Reserved	R/W	0x0
0	Status_Clear1	Status indicator clear bit write 1 to this bit, and the register bit15~7 will be cleared. after clearing, this bit turn to 1 automatically	R/W	0x0

11.4.18 PMU_DC1_CTL0

PMU_DC1_CTL0 Register （default 0x8629）
Offset = 0x11

Bit(s)	Name	Description	R/W	Reset
15：12	Reserved	Reserved	R/W	1000
11-7	DC1_VOL	DC1(vdd) Voltage setting 00000:0.700v 00001:0.725v …… 01100:1.00v …… 11100:1.40v Others:reserved DCDC1_VOLTAGE=0.7v+ DCDC1_VOL*25mv	R/W	01100
6 ： 0	Reserved	Reserved	R/W	0101001

11.4.19 PMU_DC1_CTL1

PMU_DC1_CTL1 Register （default 0xecae）
Offset = 0x12

Bit(s)	Name	Description	R/W	Reset
15 ： 0	Reserved	Reserved	R/W	1110110010101110

11.4.20 PMU_DC1_CTL2

PMU_DC1_CTL1 Register （default 0x334b）
Offset = 0x13

Bit(s)	Name	Description	R/W	Reset
15: 0	Reserved	Reserved	R/W	0011001101001011

11.4.21 PMU_DC2_CTL0

PMU_DC2_CTL0 Register （default 0x088b）
Offset = 0x14

Bit(s)	Name	Description	R/W	Reset
15	DC2_EN	DCDC2 enable	R/W	0
14-12	Reserved	Reserved	R/W	000
11-8	DC2_VOL	DCDC2Voltage setting 0000:1.30v 0001:1.35v 0010:1.40v 0011:1.45v 0100:1.50v 0101:1.55v 0110:1.60v 0111:1.65v 1000:1.70v 1001:1.75v 1010:1.80v 1011:1.85v 1100:1.90v 1101:1.95v 1110:2.05v 1111:2.15v	R/W	1000
7 ： 0	Reserved	Reserved	R/W	1000101

11.4.22 PMU_DC2_CTL1

PMU_DC2_CTL1 Register （default 0xECAE）
Offset = 0x15

Bit(s)	Name	Description	R/W	Reset
15：0	Reserved	Reserved	R/W	1110110010101110

11.4.23 PMU_DC2_CTL2

PMU_DC2_CTL1 Register （default 0x334b）

Offset = 0x16

Bit(s)	Name	Description	R/W	Reset
15: 0	Reserved	Reserved	R/W	0011001101001011

11.4.24 PMU_DC3_CTL0

PMU_DC3_CTL0 Register （default 0x8B8B）

Offset = 0x17

Bit(s)	Name	Description	R/W	Reset
15-12	Reserved	Reserved	R/W	1000
11-9	DC3_VOL	DCDC3 Voltage setting 000:2.6v 001:2.7v 010:2.8v 011:2.9v 100:3.0v 101:3.1v 110:3.2v 111:3.3v	R/W	101
8：7	EN_SETVCC	Select working circuit： 00：LDO mode work 01：DCDC mode work 1X：LDO mode work	R/W	11
6：0	Reserved	Reserved	R/W	0001011

11.4.25 PMU_DC3_CTL1

PMU_DC3_CTL1 Register （default 0xe52e）

Offset = 0x18

Bit(s)	Name	Description	R/W	Reset
15：0	Reserved	Reserved	R/W	1110010100101110

11.4.26 PMU_DC3_CTL2

PMU_DC3_CTL1 Register （default 0x334B）

Offset = 0x19

Bit(s)	Name	Description	R/W	Reset
15: 0	Reserved	Reserved	R/W	0011001100001011

11.4.27 PMU_DC4_CTL0

PMU_DC4_CTL0 Register （default 0x81f4）

Offset = 0x1A

Bit(s)	Name	Description	R/W	Reset
15：1	Reserved	Reserved	R/W	100000011111010
0	DC4_EN	DCDC4 enable bit 0：disable 1：enable	R/W	0

11.4.28 PMU_DC4_CTL1

PMU_DC4_CTL1 Register （default 0x0000）

Offset = 0x1B

Bit(s)	Name	Description	R/W	Reset
15：0	Reserved	Reserved	R/W	00

11.4.29 PMU_LDO1_CTL

PMU_LDO1_CTL Register （default 0xa000）

Offset = 0x1E

Bit(s)	Name	Description	R/W	Reset
15-13	LDO1_VOL	LDO1 Voltage setting 000:2.6v 001:2.7v 010:2.8v 011:2.9v 100:3.0v 101:3.1v 110:3.2v	R/W	101

		111:3.3v		
12-0	Reserved	Reserved	R/W	0

11.4.30 PMU_LDO2_CTL

PMU_LDO2_CTL Register （default 0xa000）
Offset = 0x1F

Bit(s)	Name	Description	R/W	Reset
15：13	LDO2_VOL	LDO2 Voltage setting 000:2.6v 001:2.7v 010:2.8v 011:2.9v 100:3.0v 101:3.1v 110:3.2v 111:3.3v	R/W	101
12：0	Reserved	Reserved	R/W	0

11.4.31 PMU_LDO3_CTL

PMU_LDO3_CTL Register （default 0x6000）
Offset = 0x20

Bit(s)	Name	Description	R/W	Reset
15：13	LDO3_VOL	LDO3 Voltage setting 000:1.5v 001:1.6v 010:1.7v 011:1.8v 100:1.9v 101:2.0v Others:Reserved	R/W	011
12：0	Reserved	Reserved	R/W	0

11.4.32PMU_LDO4_CTL

PMU_LDO4_CTL Register （default 0x6000）
Offset = 0x21

Bit(s)	Name	Description	R/W	Reset
15：13	LDO4_VOL	LDO4 Voltage setting 000:2.8v 001:2.9v 010:3.0v 011:3.1v 100:3.2v 101:3.3v 110:3.4v 111:3.5v	R/W	011
12：1	Reserved	Reserved	R/W	0
0	LDO4_EN	LDO4 enable bit 0：disable 1：enable	R/W	0

11.4.33 PMU_LDO5_CTL

PMU_LDO5_CTL Register （default 0x4000）
Offset = 0x22

Bit(s)	Name	Description	R/W	Reset
15：13	LDO5_VOL	LDO5 Voltage setting 000:2.6v 001:2.7v 010:2.8v 011:2.9v 100:3.0v 101:3.1v 110:3.2v 111:3.3v	R/W	010
12：1	Reserved	Reserved	R/W	0
0	LDO5_EN	LDO5 enable bit	R/W	0

		0：disable 1：enable		

11.4.34 PMU_LDO6_CTL

PMU_LDO6_CTL Register （default 0x6000）
Offset = 0x23

Bit(s)	Name	Description	R/W	Reset
15：11	LDO6_VOL	LDO6 Voltage setting 00000:0.700v 00001:0.725v …… 01100:1.00v …… 11100:1.40v Others:1.40v LDO6_VOLTAGE=0.7v+ LDO6_VOL*25mv	R/W	01100
10：0	Reserved	Reserved	R/W	0

11.4.35 PMU_LDO7_CTL

PMU_LDO7_CTL Register （default 0x6000）
Offset = 0x24

Bit(s)	Name	Description	R/W	Reset
15：13	LDO7_VOL	LDO7 Voltage setting 000:1.5v 001:1.6v 010:1.7v 011:1.8v 100:1.9v 101:2.0v Others:2.0v	R/W	011
12：1	Reserved	Reserved	R/W	0

0	LDO7_EN	LDO7 enable bit 0：disable 1：enable	R/W	0

11.4.36 PMU_LDO8_CTL

PMU_LDO8_CTL Register （default 0x8000）

Offset = 0x25

Bit(s)	Name	Description	R/W	Reset
15：12	LDO8_VOL	LDO8 Voltage setting 0000:2.3v 0001:2.4v 0010:2.5v 0011:2.6v 0100:2.7v 0101:2.8v 0110:2.9v 0111:3.0v 1000:3.1v 1001:3.2v 1010:3.3v Others：3.3v	R/W	1000
10：1	Reserved	Reserved	R/W	0
0	LDO8_EN	LDO8 enbale bit 0：disable 1：enable	R/W	0

11.4.37 PMU_LDO9_CTL

PMU_LDO9_CTL Register （default 0x4000）

Offset = 0x26

Bit(s)	Name	Description	R/W	Reset
15：13	LDO9_VOL	LDO9 Voltage setting 000:1.0v	R/W	010

		001:1.1v 010:1.2v 011:1.3v 100:1.4v 101:1.5v Others: 1.5v		
12：1	Reserved	Reserved	R/W	0
0	LDO9_EN	LDO9 enable bit 0：disable 1：enable	R/W	0

11.4.38 PMU_LDO10_CTL

PMU_LDO10_CTL Register （default 0x8000）

Offset = 0x27

Bit(s)	Name	Description	R/W	Reset
15：12	LDO10_VOL	LDO10 Voltage setting 0000:2.3v 0001:2.4v 0010:2.5v 0011:2.6v 0100:2.7v 0101:2.8v 0110:2.9v 0111:3.0v 1000:3.1v 1001:3.2v 1010:3.3v Others: 3.3v	R/W	1000
11：1	Reserved	Reserved	R/W	0
0	LDO10_EN	LDO10 enable bit 0：disable 1：enable	R/W	0

11.4.39 PMU_LDO11_CTL

PMU_LDO12_CTL Register （default 0xB000）
Offset = 0x28

Bit(s)	Name	Description	R/W	Reset
15：13	LDO11_VOL	LDO11 Voltage setting 000:2.6v 001:2.7v 010:2.8v 011:2.9v 100:3.0v 101:3.1v 110:3.2v 111:3.3v	R/W	101
12	SVCC_LOW_EN	SVCC low-power protection enable 0：Disable 1：Enable	R/W	1
11：0	Reserved	Reserved	R/W	0

11.4.40 PMU_SWITCH_CTL

PMU_SWITCH_CTL Register （default 0x0000）
Offset = 0x29

Bit(s)	Name	Description	R/W	Reset
15	SWITCH1_EN	SWITCH1_EN 0：disable 1：enable	R/W	0
14	SWITCH2_EN	SWITCH2_EN 0：disable 1：enable when the bit is 1，SWITCH2 opened,; when it is 0, it closed.	R/W	0
13	SWITCH2_MOD	SWITCH2 mode selection 0：SWITCH 1：LDO When the bit is 0， SWITCH2 is used as switch;	R/W	0

		when it is 1，it used as LDO		
12	SWITCH2_LDO_VOL_sel	SWITCH2 used as LDO, voltage step serring 0：output is 1.0~2.0v 1：output is 2.3~3.3v	R/W	0
11：8	SWITCH2_LDO_VOL	SWITCH2 used as LDO, the voltage setting 0000：1.0v 2.3v 0001：1.1v 2.4v 0010：1.2v 2.5v 0011：1.3v 2.6v 0100：1.4v 2.7v 0101：1.5v 2.8v 0110：1.6v 2.9v 0111：1.7v 3.0v 1000：1.75v 3.05v 1001：1.8v 3.1v 1010：1.85v 3.15v 1011：1.9v 3.2v 1100：1.95v 3.25v 1101：2.0v 3.3v Others：2.0v 3.3v	R/W	0000
7：6	Reserved	Reserved	R/W	0
5	SWITCH1_MODE	SWITCH1 mode selection 0：SWITCH 1：LDO When bit is 0，SWITCH1 is used as switch, when it is 1，it used as LDO	R/W	0
4：3	SWITCH1_LDO_VOL	SWITCH1 used as LDO, the voltage setting 00：3.0v 01：3.1v 10：3.2v 11：3.3v	R/W	00
2	Reserved	Reserved	R/W	0
1	SWITCH1_Discharge_EN	SWITCH1 discharge enable control 0：Disbale 1：Enable Bit1 and bit2 cannot be 1 at the same time；Bit1 and bit15 cannot be 1 at the same time.	R/W	0
0	Reserved	Reserved	R/W	0

11.4.41 PMU_OV_CTL0

PMU_OV_CTL0 Register （default 0x5555）
Offset = 0x2A

Bit(s)	Name	Description	R/W	Reset
15	Reserved	Reserved	R/W	0
14	DCDC1_OV_Set	DCDC1 output overvoltage setting 0：10% DC1OUT 1：20% DC1OUT If detecting DC1OUT voltage is higher than its setting more than 1ms, and its corresponding enable bit is 1, it will send out DCDC1 overvoltage suspend.	R/W	1
13	Reserved	Reserved	R/W	0
12	DCDC2_OV_Set	DCDC2 output overvoltage setting 0：10% DC2OUT 1：20% DC2OUT If detecting DC2OUT voltage is higher than its setting more than 1ms, and its corresponding enable bit is 1, it will send out DCDC2 overvoltage suspend.	R/W	1
11	Reserved	Reserved	R/W	0
10	DCDC3_OV_Set	DCDC3 output overvoltage setting 0：10% DC3OUT 1：20% DC3OUT If detecting DC3OUT voltage is higher than its setting more than 1ms, and its corresponding enable bit is 1, it will send out DCDC3 overvoltage suspend.	R/W	1
9-8	DCDC4_OV_Set	DCDC4 output overvoltage setting 00：5% DC4OUT 01：10% DC4OUT 10：15% DC4OUT 11：20% DC4OUT If detecting DC4OUT voltage is higher than its setting more than 1ms,	R/W	01

		and its corresponding enable bit is 1, it will send out DCDC4 overvoltage suspend.		
7-6	LDO1_OV_Set	LDO1 output overvoltage setting 00：7% LDO1OUT 01：11% LDO1OUT 10：15% LDO1OUT 11：20% LDO1OUT If detecting LDO1OUT voltage is higher than its setting more than 1ms, and its corresponding enable bit is 1, it will send out LDO1 overvoltage suspend.	R/W	01
5-4	LDO2_OV_Set	LDO2 output overvoltage setting 00：5% LDO2OUT 01：10% LDO2OUT 10：15% LDO2OUT 11：20% LDO2OUT If detecting LDO2OUT voltage is higher than its setting more than 1ms, and its corresponding enable bit is 1, it will send out LDO2 overvoltage suspend..	R/W	01
3-2	LDO3_OV_Set	LDO3 output overvoltage setting 00：5% LDO3OUT 01：10% LDO3OUT 10：15% LDO3OUT 11：20% LDO3OUT If detecting LDO3OUT voltage is higher than its setting more than 1ms, and its corresponding enable bit is 1, it will send out LDO3 overvoltage suspend..	R/W	01
1-0	LDO4_OV_Set	LDO4 output overvoltage setting 00：5% LDO4OUT 01：10% LDO4OUT 10：15% LDO4OUT 11：20% LDO4OUT If detecting LDO4OUT voltage is higher than its setting more than 1ms,	R/W	01

		and its corresponding enable bit is 1, it will send out LDO4 overvoltage suspend..		

11.4.42 PMU_OV_CTL1

PMU_OV_CTL1 Register （default 0x5550）
Offset = 0x2B

Bit(s)	Name	Description	R/W	Reset
15-14	LDO5_OV_Set	LDO5 output overvoltage setting 00：5% LDO5OUT 01：10% LDO5OUT 10：15% LDO5OUT 11：20% LDO5OUT If detecting LDO5OUT voltage is higher than its setting more than1ms, and its corresponding enable bit is 1, it will send out LDO5 overvoltage suspend..	R/W	01
13-12	LDO6_OV_Set	LDO6 output overvoltage setting 00：5% LDO6OUT 01：10% LDO6OUT 10：15% LDO6OUT 11：20% LDO6OUT If detecting LDO6OUT voltage is higher than its setting more than 1ms, and its corresponding enable bit is 1, it will send out LDO6 overvoltage suspend.	R/W	01
11-10	LDO7_OV_Set	LDO7 output overvoltage setting 00：5% LDO7OUT 01：10% LDO7OUT 10：15% LDO7OUT 11：20% LDO7OUT If detecting LDO7OUT voltage is higher than its setting more than 1ms, and its corresponding enable bit is 1, it will send out LDO7	R/W	01

		overvoltage suspend.		
9-8	LDO8_OV_Set	LDO8 output overvoltage setting 00：5% LDO8OUT 01：10% LDO8OUT 10：15% LDO8OUT 11：20% LDO8OUT If detecting LDO8OUT voltage is higher than its setting more than 1ms, and its corresponding enable bit is 1, it will send out LDO8 overvoltage suspend.	R/W	01
7-6	LDO9_OV_Set	LDO9 output overvoltage setting 00：5% LDO9OUT 01：10% LDO9OUT 10：15% LDO9OUT 11：20% LDO9OUT If detecting LDO9OUT voltage is higher than its setting more than 1ms, and its corresponding enable bit is 1, it will send out LDO9 overvoltage suspend.	R/W	01
5-4	LDO10_OV_Set	LDO10 output overvoltage setting 00：5% LDO10OUT 01：10% LDO10OUT 10：15% LDO10OUT 11：20% LDO10OUT If detecting LDO10OUT voltage is higher than its setting more than 1ms, and its corresponding enable bit is 1, it will send out LDO10 overvoltage suspend	R/W	01
3-0	Reserved	Reserved	R/W	0

11.4.43 PMU_OV_Status

PMU_OV_Status Register （default 0x0000）

Offset = 0x2C

Bit(s)	Name	Description	R/W	Reset

15	DCDC1_OV_STATUS	DCDC1 output overvoltage state indication 0： not overvoltage is detected in DCDC1 1：vervoltage is detected in DCDC1	R	0
14	DCDC2_OV_STATUS	DCDC2 output overvoltage state indication 0： not overvoltage is detected in DCDC2 1：vervoltage is detected in DCDC2	R	0
13	DCDC3_OV_STATUS	DCDC3 output overvoltage state indication 0： not overvoltage is detected in DCDC3 1：vervoltage is detected in DCDC3	R	0
12	DCDC4_OV_STATUS	DCDC4 output overvoltage state indication 0： not overvoltage is detected in DCDC4 1：vervoltage is detected in DCDC4	R	0
11	LDO1_OV_STATUS	LDO1 output overvoltage state indication 0：not overvoltage is detected in LDO1 1：vervoltage is detected in LDO1	R	0
10	LDO2_OV_STATUS	LDO2 output overvoltage state indication 0：not overvoltage is detected in LDO2 1：vervoltage is detected in LDO2	R	0
9	LDO3_OV_STATUS	LDO3 output overvoltage state indication 0：not overvoltage is detected in LDO3 1：vervoltage is detected in LDO3	R	0
8	LDO4_OV_STATUS	LDO4 output overvoltage state indication 0：not overvoltage is detected in LDO4 1：vervoltage is detected in LDO4	R	0
7	LDO5_OV_STATUS	LDO5 output overvoltage state indication 0：not overvoltage is detected in LDO5 1：vervoltage is detected in LDO5	R	0

6	LDO6_OV_STATUS	LDO6 output overvoltage state indication 0：not overvoltage is detected in LDO6 1：vervoltage is detected in LDO6	R	0
5	LDO7_OV_STATUS	LDO7 output overvoltage state indication 0：not overvoltage is detected in LDO7 1：vervoltage is detected in LDO7	R	0
4	LDO8_OV_STATUS	LDO8 output overvoltage state indication 0：not overvoltage is detected in LDO8 1：vervoltage is detected in LDO8	R	0
3	LDO9_OV_STATUS	LDO9 output overvoltage state indication 0：not overvoltage is detected in LDO9 1：vervoltage is detected in LDO9	R	0
2	LDO10_OV_STATUS	LDO10 output overvoltage state indication 0：not overvoltage is detected in LDO10 1：vervoltage is detected in LDO10	R	0
1	Reserved	Reserved	R/W	0
0	Status_Clear2	State indicates to clear bit Write 1 to this bit, it will clear bit15~2 of this register, after that, this bit turns to 0 automatically	R/W	0x0

11.4.44 PMU_OV_EN

PMU_OV_EN Register （default 0xFFFC）

Offset = 0x2D

Bit(s)	Name	Description	R/W	Reset
15	DCDC1_OV_EN	DCDC1 output overvoltage detect enable 0：Disable 1：Enable	R/W	1
14	DCDC2_OV _EN	DCDC2 output overvoltage detect enable	R/W	1

		0：Disable 1：Enable		
13	DCDC3_OV _EN	DCDC3 output overvoltage detect enable 0：Disable 1：Enable	R/W	1
12	DCDC4_OV _EN	DCDC4 output overvoltage detect enable 0：Disable 1：Enable	R/W	1
11	LDO1_OV _EN	LDO1 output overvoltage detect enable 0：Disable 1：Enable	R/W	1
10	LDO2_OV _EN	LDO2 output overvoltage detect enable 0：Disable 1：Enable	R/W	1
9	LDO3_OV _EN	LDO3 output overvoltage detect enable 0：Disable 1：Enable	R/W	1
8	LDO4_OV _EN	LDO4 output overvoltage detect enable 0：Disable 1：Enable	R/W	1
7	LDO5_OV _EN	LDO5 output overvoltage detect enable 0：Disable 1：Enable	R/W	1
6	LDO6_OV_EN	LDO6 output overvoltage detect enable 0：Disable 1：Enable	R/W	1
5	LDO7_OV _EN	LDO7 output overvoltage detect enable 0：Disable 1：Enable	R/W	1
4	LDO8_OV _EN	LDO8 output overvoltage detect enable 0：Disable 1：Enable	R/W	1
3	LDO9_OV _EN	LDO9 output overvoltage detect enable 0：Disable 1：Enable	R/W	1
2	LDO10_OV _EN	LDO10 output overvoltage detect enable 0：Disable	R/W	1

		1：Enable		
1:0	Reserved	Reserved	R/W	0

11.4.45 PMU_OV_INT_EN

PMU_OV_INT_EN Register （default 0xFFFC）
Offset = 0x2E

Bit(s)	Name	Description	R/W	Reset
15	DCDC1_OV_INT_EN	DCDC1 output overvoltage detect enable 0：Disable 1：Enable	R/W	1
14	DCDC2_OV_INT _EN	DCDC2 output overvoltage detect enable 0：Disable 1：Enable	R/W	1
13	DCDC3_OV_INT _EN	DCDC3 output overvoltage detect enable 0：Disable 1：Enable	R/W	1
12	DCDC4_OV_INT _EN	DCDC4 output overvoltage detect enable 0：Disable 1：Enable	R/W	1
11	LDO1_OV_INT _EN	LDO1 output overvoltage detect enable 0：Disable 1：Enable	R/W	1
10	LDO2_OV_INT _EN	LDO2 output overvoltage detect enable 0：Disable 1：Enable	R/W	1
9	LDO3_OV_INT _EN	LDO3 output overvoltage detect enable 0：Disable 1：Enable	R/W	1
8	LDO4_OV_INT _EN	LDO4 output overvoltage detect enable 0：Disable 1：Enable	R/W	1
7	LDO5_OV_INT _EN	LDO5 output overvoltage detect enable 0：Disable	R/W	1

		1：Enable		
6	LDO6_O_INT V_EN	LDO6 output overvoltage detect enable 0：Disable 1：Enable	R/W	1
5	LDO7_OV_INT _EN	LDO7 output overvoltage detect enable 0：Disable 1：Enable	R/W	1
4	LDO8_OV_INT _EN	LDO8 output overvoltage detect enable 0：Disable 1：Enable	R/W	1
3	LDO9_OV_INT _EN	LDO9 output overvoltage detect enable 0：Disable 1：Enable	R/W	1
2	LDO10_OV_INT _EN	LDO10 output overvoltage detect enable 0：Disable 1：Enable	R/W	1
1:0	Reserved	Reserved	R/W	0

11.4.46 PMU_OC_CTL

PMU_OV_CTL Register （default 0x0000）

Offset = 0x2F

Bit(s)	Name	Description	R/W	Reset
15	LDO1_OC_Set	LDO1 output overcurrent setting 0：800mA 1：900mA If LDO1 comes up overcurrent, then entering standby directly	R/W	0
14	LDO2_OC_Set	LDO2 output overcurrent setting 0：400mA 1：500mA If LDO2 comes up overcurrent, then entering standby directly	R/W	0
13	LDO3_OC_Set	LDO3 output overcurrent setting 0：500mA 1：600mA If LDO3 comes up overcurrent, then	R/W	0

		entering standby directly		
12	LDO4_OC_Set	LDO4 output overcurrent setting 0：800mA 1：900mA If detecting LDO4OUT output current is beyond its setting, and its corresponding suspend is enable, it will be interrupt, and close this LDO. To restart the LDO,must disable first and then Enable again,or disable the overcurrent detect of the LDO.	R/W	0
11	LDO5_OC_Set	LDO5 output overcurrent setting 0：300mA 1：400mA If detecting LDO5OUT output current is beyond its setting, and its corresponding suspend is enable, it will be interrupt, and close this LDO. To restart the LDO,must disable first and then enable again,or disable the overcurrent detect of the LDO	R/W	0
10	LDO6_OC_Set	LDO6 output overcurrent setting 0：400mA 1：500mA If LDO6 come up overcurrent, then entering Standby mode directly.	R/W	0
9	LDO7_OC_Set	LDO7 output overcurrent setting 0：400mA 1：500mA If detecting LDO7OUT output current is beyond its setting, and its corresponding suspend is enable, it will be interrupt, and close this LDO. To restart the LDO,must disable first and then enable again,or disable the overcurrent detect of the LDO	R/W	0
8	LDO8_OC_Set	LDO8 output overcurrent setting 0：300mA 1：400mA If detecting LDO8OUT output current	R/W	0

		is beyond its setting, and its corresponding suspend is enable, it will be interrupt, and close this LDO. To restart the LDO,must disable first and then enable again,or disable the overcurrent detect of the LDO		
7	LDO9_OC_Set	LDO9 output overcurrent setting 0：300mA 1：400mA If detecting LDO9OUT output current is beyond its setting, and its corresponding suspend is enable, it will be interrupt, and close this LDO. To restart the LDO,must disable first and then enable again,or disable the overcurrent detect of the LDO	R/W	0
6	LDO10_OC_Set	LDO10 output overcurrent setting 0：300mA 1：400mA If detecting LDO10OUT output current is beyond its setting, and its corresponding suspend is enable, it will be interrupt, and close this LDO. To restart the LDO,must disable first and then enable again,or disable the overcurrent detect of the LDO	R/W	0
5:0	Reserved	Reserved	R/W	0

11.4.47 PMU_OC_Status

PMU_OC_Status Register （default 0x0000）
Offset = 0x30

Bit(s)	Name	Description	R/W	Reset
15	LDO1_OC_STATUS	LDO1 output overcurrent state indication 0：not overcurrentis detected in LDO1 1：overcurrent is detected in LDO1 After LDO overcurrent, hardware	R	0

		shutoff this LDO, and set 1 to this bit.		
14	LDO2_OC_STATUS	LDO2 output overcurrent state indication 0：not overcurrentis detected in LDO2 1：overcurrent is detected in LDO2 After LDO overcurrent, hardware shutoff this LDO, and set 1 to this bit.	R	0
13	LDO3_OC_STATUS	LDO3 output overcurrent state indication 0：not overcurrentis detected in LDO3 1：overcurrent is detected in LDO3 After LDO overcurrent, hardware shutoff this LDO, and set 1 to this bit.	R	0
12	LDO4_OC_STATUS	LDO4 output overcurrent state indication 0：not overcurrentis detected in LDO4 1：overcurrent is detected in LDO4 After LDO overcurrent, hardware shutoff this LDO, and set 1 to this bit.	R	0
11	LDO5_OC_STATUS	LDO5 output overcurrent state indication 0：not overcurrentis detected in LDO5 1：overcurrent is detected in LDO5 After LDO overcurrent, hardware shutoff this LDO, and set 1 to this bit.	R	0
10	LDO6_OC_STATUS	LDO6 output overcurrent state indication 0：not overcurrentis detected in LDO6 1：overcurrent is detected in LDO6 After LDO overcurrent, hardware shutoff this LDO, and set 1 to this bit.	R	0
9	LDO7_OC_STATUS	LDO7 output overcurrent state indication 0：not overcurrentis detected in LDO7 1：overcurrent is detected in LDO7 After LDO overcurrent, hardware shutoff this LDO, and set 1 to this bit.	R	0
8	LDO8_OC_STATUS	LDO8 output overcurrent state indication 0：not overcurrentis detected in LDO8	R	0

		1：overcurrent is detected in LDO8 After LDO overcurrent, hardware shutoff this LDO, and set 1 to this bit.		
7	LDO9_OC_STATUS	LDO9 output overcurrent state indication 0：not overcurrentis detected in LDO9 1：overcurrent is detected in LDO9 After LDO overcurrent, hardware shutoff this LDO, and set 1 to this bit.	R	0
6	LDO10_OC_STATUS	LDO10 output overcurrent state indication 0：not overcurrentis detected in LDO10 1：overcurrent is detected in LDO10 After LDO overcurrent, hardware shutoff this LDO, and set 1 to this bit.	R	0
5:1	Reserved	Reserved	R/W	0
0	Status_Clear3	State indication clear bit Write 1 to this bit, then clear bit15~2 of this register, after clearing, the bit turns to 0	R/W	0x0

11.4.48 PMU_OC_EN

PMU_OC_EN Register （default 0Xffc0）

Offset = 0x31

Bit(s)	Name	Description	R/W	Reset
15	LDO1_OC_EN	LDO1 output overcurrent detect enable 0：Disable 1：Enable	R/W	1
14	LDO2_OC_EN	LDO2 output overcurrent detect enable 0：Disable 1：Enable	R/W	1
13	LDO3_OC_EN	LDO3 output overcurrent detect enable 0：Disable 1：Enable	R/W	1
12	LDO4_OC_EN	LDO4 output overcurrent detect enable 0：Disable 1：Enable	R/W	1

11	LDO5_OC_EN	LDO5 output overcurrent detect enable 0：Disable 1：Enable	R/W	1
10	LDO6_OC_EN	LDO6 output overcurrent detect enable 0：Disable 1：Enable	R/W	1
9	LDO7_OC_EN	LDO7 output overcurrent detect enable 0：Disable 1：Enable	R/W	1
8	LDO8_OC_EN	LDO8 output overcurrent detect enable 0：Disable 1：Enable	R/W	1
7	LDO9_OC_EN	LDO9 output overcurrent detect enable 0：Disable 1：Enable	R/W	1
6	LDO10_OC_EN	LDO10 output overcurrent detect enable 0：Disable 1：Enable	R/W	1
5:0	Reserved	Reserved	R/W	0

11.4.49 PMU_OC_INT_EN

PMU_OC_INT_EN Register （default 0x1bc0）

Offset = 0x32

Bit(s)	Name	Description	R/W	Reset
15：13	Reserved	Reserved	R/W	0
12	LDO4_OC_INT _EN	LDO4 output overcurrent suspend enable 0：Disable 1：Enable	R/W	1
11	LDO5_OC_INT _EN	LDO5 output overcurrent suspend enable 0：Disable 1：Enable	R/W	1
10	Reserved	Reserved	R/W	0
9	LDO7_OC_INT _EN	LDO7 output overcurrent suspend enable	R/W	1

		0：Disable 1：Enable		
8	LDO8_OC_INT _EN	LDO8 output overcurrent suspend enable 0：Disable 1：Enable	R/W	1
7	LDO9_OC_INT _EN	LDO9 output overcurrent suspend enable 0：Disable 1：Enable	R/W	1
6	LDO10_OC_INT _EN	LDO9 output overcurrent suspend enable 0：Disable 1：Enable	R/W	1
5:0	Reserved	Reserved	R/W	0

11.4.50 PMU_UV_CTL0

PMU_UV_CTL0 Register （default 0x5555）
Offset = 0x33

Bit(s)	Name	Description	R/W	Reset
15	Reserved	Reserved	R/W	0
14	DCDC1_UV_Set	DCDC1 output undervoltage setting 0：10% DC1OUT 1：20% DC1OUT If detecting DC1OUT voltage is lower than the settings more than 1ms, and its corresponding enable bit is 1，DCDC1 undervoltage suspend will be sent out.	R/W	1
13	Reserved	Reserved	R/W	0
12	DCDC2_UV_Set	DCDC2 output undervoltage setting 0：10% DC2OUT 1：20% DC2OUT If detecting DC2OUT voltage is lower than the settings more than 1ms, and its corresponding enable bit is 1，DCDC2 undervoltage suspend	R/W	1

		will be sent out.		
11	Reserved	Reserved	R/W	0
10	DCDC3_UV_Set	DCDC3 output undervoltage setting 0：10% DC3OUT 1：20% DC3OUT If detecting DC3OUT voltage is lower than the settings more than 1ms, and its corresponding enable bit is 1，DCDC3 undervoltage suspend will be sent out.	R/W	1
9-8	DCDC4_UV_Set	DCDC4 output undervoltage setting 00：5% DC4OUT 01：10% DC4OUT 10：15% DC4OUT 11：20% DC4OUT If detecting DC4OUT voltage is lower than the settings more than 1ms, and its corresponding enable bit is 1，DCDC4 undervoltage suspend will be sent out.	R/W	01
7-6	LDO1_UV_Set	LDO1 output undervoltage setting 00：5% LDO1OUT 01：10% LDO1OUT 10：15% LDO1OUT 11：20% LDO1OUT If detecting LDO1OUT voltage is lower than the settings more than 1ms, and its corresponding enable bit is 1，LDO1 undervoltage suspend will be sent out. R/W	R/W	01
5-4	LDO2_UV_Set	LDO2 output undervoltage setting 00：5% LDO2OUT 01：10% LDO2OUT 10：15% LDO2OUT 11：20% LDO2OUT If detecting LDO2OUT voltage is lower than the settings more than 1ms, and its corresponding enable bit is 1，LDO2 undervoltage suspend will be sent out.	R/W	01

3-2	LDO3_UV_Set	LDO3 output undervoltage setting 00：5% LDO3OUT 01：10% LDO3OUT 10：15% LDO3OUT 11：20% LDO3OUT If detecting LDO3OUT voltage is lower than the settings more than 1ms, and its corresponding enable bit is 1，LDO3 undervoltage suspend will be sent out.	R/W	01
1-0	LDO4_UV_Set	LDO4 output undervoltage setting 00：5% LDO4OUT 01：10% LDO4OUT 10：15% LDO4OUT 11：20% LDO4OUT If detecting LDO4OUT voltage is lower than the settings more than 1ms, and its corresponding enable bit is 1，LDO4 undervoltage suspend will be sent out.	R/W	01

11.4.51 PMU_UV_CTL1

PMU_UV_CTL1 Register （default 0x5550）

Offset = 0x34

Bit(s)	Name	Description	R/W	Reset
15-14	LDO5_UV_Set	LDO5 output undervoltage setting 00：5% LDO5OUT 01：10% LDO5OUT 10：15% LDO5OUT 11：20% LDO5OUT If detecting LDO5OUT voltage is lower than the settings more than 1ms, and its corresponding enable bit is 1，LDO5 undervoltage suspend will be sent out.	R/W	01
13-12	LDO6_UV_Set	LDO6 output undervoltage setting 00：5% LDO6OUT	R/W	01

		01：10% LDO6OUT 10：15% LDO6OUT 11：20% LDO6OUT If detecting LDO6OUT voltage is lower than the settings more than 1ms, and its corresponding enable bit is 1，LDO6 undervoltage suspend will be sent out.		
11-10	LDO7_UV_Set	LDO7 output undervoltage setting 00：5% LDO7OUT 01：10% LDO7OUT 10：15% LDO7OUT 11：20% LDO7OUT If detecting LDO7OUT voltage is lower than the settings more than 1ms, and its corresponding enable bit is 1，LDO7 undervoltage suspend will be sent out.	R/W	01
9-8	LDO8_UV_Set	LDO8 output undervoltage setting 00：5% LDO8OUT 01：10% LDO8OUT 10：15% LDO8OUT 11：20% LDO8OUT If detecting LDO8OUT voltage is lower than the settings more than 1ms, and its corresponding enable bit is 1，LDO8 undervoltage suspend will be sent out.	R/W	01
7-6	LDO9_UV_Set	LDO9 output undervoltage setting 00：5% LDO9OUT 01：10% LDO9OUT 10：15% LDO9OUT 11：20% LDO9OUT If detecting LDO9OUT voltage is lower than the settings more than 1ms, and its corresponding enable bit is 1，LDO9 undervoltage suspend will be sent out.	R/W	01
5-4	LDO10_UV_Set	LDO10 output undervoltage setting 00：5% LDO10OUT	R/W	01

		01：10% LDO10OUT 10：15% LDO10OUT 11：20% LDO10OUT If detecting LDO10OUT voltage is lower than the settings more than 1ms, and its corresponding enable bit is 1，LDO10 undervoltage suspend will be sent out.		
3-0	Reserved	Reserved	R/W	0

11.4.52 PMU_UV_Status

PMU_UV_Status Register （default 0x0000）
Offset = 0x35

Bit(s)	Name	Description	R/W	Reset
15	DCDC1_UV_STATUS	DCDC1 output undervoltage state indication 0：not undervoltage detected in DCDC1 1：undervoltageis detected in DCDC1	R	0
14	DCDC2_UV_STATUS	DCDC2 output undervoltage state indication 0：not undervoltage detected in DCDC2 1：undervoltageis detected in DCDC2	R	0
13	DCDC3_UV_STATUS	DCDC3 output undervoltage state indication 0：not undervoltage detected in DCDC3 1：undervoltageis detected in DCDC3	R	0
12	DCDC4_UV_STATUS	DCDC4 output undervoltage state indication 0：not undervoltagedetected in DCDC4 1：undervoltageis detected in DCDC4	R	0

11	LDO1_UV_STATUS	LDO1 output undervoltage state indication 0：not undervoltage detected in LDO1 1：undervoltageis detected in LDO1	R	0
10	LDO2_UV_STATUS	LDO2 output undervoltage state indication 0：not undervoltage detected in LDO2 1：undervoltageis detected in LDO2	R	0
9	LDO3_UV_STATUS	LDO3 output undervoltage state indication 0：not undervoltage detected in LDO3 1：undervoltageis detected in LDO3	R	0
8	LDO4_UV_STATUS	LDO4 output undervoltage state indication 0：not undervoltage detected in LDO4 1：undervoltageis detected in LDO4	R	0
7	LDO5_UV_STATUS	LDO5 output undervoltage state indication 0：not undervoltagedetected in LDO5 1：undervoltageis detected in LDO5	R	0
6	LDO6_UV_STATUS	LDO6 output undervoltage state indication 0：not undervoltage detected in LDO6 1：undervoltageis detected in LDO6	R	0
5	LDO7_UV_STATUS	LDO7 output undervoltage state indication 0：not undervoltage detected in LDO7 1：undervoltageis detected in LDO7	R	0
4	LDO8_UV_STATUS	LDO8 output undervoltage state indication 0：not undervoltage detected in LDO8 1：undervoltageis detected in LDO8	R	0

3	LDO9_UV_STATUS	LDO9 output undervoltage state indication 0：not undervoltage detected in LDO9 1：undervoltageis detected in LDO9	R	0
2	LDO10_UV_STATUS	LDO10 output undervoltage state indication 0：not undervoltage detected in LDO10 1：undervoltageis detected in LDO10	R	0
1	Reserved	Reserved	R/W	0
0	Status_Clear4	State indication clear bit Write 1 to this bit, then clear bit15~2 of this register, after clearing, the bit turns to 0	R/W	0x0

11.4.53 PMU_UV_EN

PMU_UV_EN Register （default 0xFFFC）

Offset = 0x36

Bit(s)	Name	Description	R/W	Reset
15	DCDC1_UV_EN	DCDC1 output undervoltage detect enable 0：Disable 1：Enable	R/W	1
14	DCDC2_UV_EN	DCDC2 output undervoltage detect enable 0：Disable 1：Enable	R/W	1
13	DCDC3_UV_EN	DCDC3 output undervoltage detect enable 0：Disable 1：Enable	R/W	1
12	DCDC4_UV_EN	DCDC4 output undervoltage detect enable 0：Disable 1：Enable	R/W	1
11	LDO1_UV_EN	LDO1 output undervoltage detect	R/W	1

		enable 0：Disable 1：Enable		
10	LDO2_UV_EN	LDO2 output undervoltage detect enable 0：Disable 1：Enable	R/W	1
9	LDO3_UV_EN	LDO3 output undervoltage detect enable 0：Disable 1：Enable	R/W	1
8	LDO4_UV_EN	LDO4 output undervoltage detect enable 0：Disable 1：Enable	R/W	1
7	LDO5_UV_EN	LDO5 output undervoltage detect enable 0：Disable 1：Enable	R/W	1
6	LDO6_UV_EN	LDO6 output undervoltage detect enable 0：Disable 1：Enable	R/W	1
5	LDO7_UV_EN	LDO7 output undervoltage detect enable 0：Disable 1：Enable	R/W	1
4	LDO8_UV_EN	LDO8 output undervoltage detect enable 0：Disable 1：Enable	R/W	1
3	LDO9_UV_EN	LDO9 output undervoltage detect enable 0：Disable 1：Enable	R/W	1
2	LDO10_UV_EN	LDO10 output undervoltage detect enable 0：Disable 1：Enable	R/W	1
1-0	Reserved	Reserved	R/W	0

11.4.54 PMU_UV_INT_EN

PMU_UV_INT_EN Register （default 0xFFFC）
Offset = 0x37

Bit(s)	Name	Description	R/W	Reset
15	DCDC1_UV_EN	DCDC1 output undervoltage suspend enable 0：Disable 1：Enable	R/W	1
14	DCDC2_UV_EN	DCDC2 output undervoltage suspend enable 0：Disable 1：Enable	R/W	1
13	DCDC3_UV_EN	DCDC3 output undervoltage suspend enable 0：Disable 1：Enable	R/W	1
12	DCDC4_UV_EN	DCDC4 output undervoltage suspend enable 0：Disable 1：Enable	R/W	1
11	LDO1_UV_EN	LDO1 output undervoltage suspend enable 0：Disable 1：Enable	R/W	1
10	LDO2_UV_EN	LDO2 output undervoltage suspend enable 0：Disable 1：Enable	R/W	1
9	LDO3_UV_EN	LDO3 output undervoltage suspend enable 0：Disable 1：Enable	R/W	1
8	LDO4_UV_EN	LDO4 output undervoltage suspend enable 0：Disable 1：Enable	R/W	1

7	LDO5_UV_EN	LDO5 output undervoltage suspend enable 0：Disable 1：Enable	R/W	1
6	LDO6_UV_EN	LDO6 output undervoltage suspend enable 0：Disable 1：Enable	R/W	1
5	LDO7_UV_EN	LDO7 output undervoltage suspend enable 0：Disable 1：Enable	R/W	1
4	LDO8_UV_EN	LDO8 output undervoltage suspend enable 0：Disable 1：Enable	R/W	1
3	LDO9_UV_EN	LDO9 output undervoltage suspend enable 0：Disable 1：Enable	R/W	1
2	LDO10_UV_EN	LDO10output undervoltage suspend enable 0：Disable 1：Enable	R/W	1
1-0	Reserved	Reserved	R/W	0

11.4.55 PMU_OT_CTL

PMU_OT_CTL Register （default 0x3B00）
Offset = 0x38

Bit(s)	Name	Description	R/W	Reset
15	OT_Status	IC overtemperature stae indication 0：not overtempreture detected 1：overtempreture detected write 1 clear 0	R/W	0
14:13	OT_Set	IC overtemperature suspend temperature setting 00：100	R/W	01

		01：120 10：130 11：140		
12	OT_INT_EN	ICovertemperature suspend enable 0：disable 1：enable	R/W	1
11	OT_SHUTOFF_EN	IC overtemperature shutoff enable 0：disable 1：enable	R/W	1
10:9	OT_SHUTOFF_Set	IC overtemperature shutoff temperature setting 00： 110 01： 130 10： 150 11： 160	R/W	01
8	OT_EN	IC overtemperature detect enable 0：disable 1：enable	R/W	1
7-0	Reserved	Reserved	R/W	0

11.4.56 PMU_CHARGER_CTL0

PMU_CHARGER_CTL0 Register （default 0x325B）

Offset = 0x39

Bit(s)	Name	Description	R/W	Reset
15	ENCH	Enable Charge Circuit 1: Enable charge circuit 0: Disable charge circuit.	R/W	0
14：10	Reserved	Reserved	R/W	01100
9	TRICKLEEN	Enable Trickle charge 0: disable 1: enable If this bit is 0,there is no Pre-charging phase, and battery charging goes to Constant current directly.	R/W	1
8：0	Reserved	Reserved	R/W	001011011

11.4.57 PMU_CHARGER_CTL1

PMU_CHARGER_CTL1 Register （default 0x0040）
Offset = 0x3A

Bit(s)	Name	Description	R/W	Reset
15	CHGEND	Charging end Status. 0: not charging over 1: charging over. If battery is not full, this bit is 0; If battery is full, this bit is 1.	R	x
14：8	Reserved	Reserved	R	x
7：4	Reserved	Reserved	R/W	0100
3:0	ICHG_REG_CC	Charge constant current charge Current Configure 0000:50mA 0001:100mA 0010:200mA 0011:300mA 0100:400mA 0101:500mA 0110:600mA 0111:700mA 1000:800mA 1001:900mA 1010:1000mA 1011:1100mA 1100:1200mA 1101:1300mA 1110:1400mA 1111:1500mA	R/W	0000

11.4.58 PMU_CHARGER_CTL2

PMU_CHARGER_CTL1 Register （default 0x0000）
Offset = 0x3B

Bit(s)	Name	Description	R/W	Reset
15：6	reserved	Reserved	R/W	0

5：4	ICHG_REG_T	Charge trickle charge Current Configure 00:50mA 01:100mA 10:200mA 11:300mA	R/W	00
3：0	Reserved	Reserved	R/W	00

11.4.59 PMU_BakCHARGER_CTL

PMU_BakCHARGER_CTL0 Register （default 0x2000）
Offset = 0x3C

Bit(s)	Name	Description	R/W	Reset
15	BK_CHGEND	Charging end Status. 0: not charging over 1: charging over. If battery is not full, this bit is 0; If battery is full, this bit is 1.	R	x
14:12	BK_CHGIS	BAK charger Current set 000：1mA 001：5mA 010：10mA 011：25mA 100：50mA Others：Reserved	R/W	010
11	BK_VOL	BAK CHARGER STOPV 0: 4.2V 1: 3V	R/W	0
10	BK_CHG_EN	BAK CHARGER ENBALE 0: DISABLE 1: ENABLE	R/W	0
9:0	reserved	Reserved	R/W	0

11.4.60 PMU_APDS_CTL

PMU_APDS_CTL0 Register （default 0x15f8）
Offset = 0x3D

Bit(s)	Name	Description	R/W	Reset
15	VBUS_CONTROL_EN	VBUS voltage current control 0：enable 1：disable After enable this bit，the system will be adjust current which is extract from VBUS automatically,. In basis of the setting of bit14，to ensure VBUS voltage is over the bit[11:10] threshold or make sure the extracted current from VBUS lower than bit[13:12] setting. Disable means to ensure the system's power current prior. If enable this bit, bit8 is invalid.	R/W	0
14	VBUS_CONTROL_SEL	VBUS control mode selection 0 voltage-limiting 1 current-limiting	R/W	0
13:12	VBUS_CUR_ Limited	VBUS current-limiting threshold current 00：100mA 01：300mA 10：500mA 11：800mA	R/W	01
11:10	VBUS_VOL_ Limited	VBUS voltage-limiting threshold voltage 00：4.2v 01：4.3v 10：4.4v 11：4.5v	R/W	01
9	VBUS_OTG	USB as OTG，VBUS supply power for the drive, when it does this, it needs to write 1 to VBUS_OTG to avoid VBUS supplying power to SYSPWR. 0 ： don't close ID from VBUS to SYSPWR 1： close ID from VBUS to SYSPWR Cut off VBUS and SYSPWR	R/W	0
8	VBUS_FST_ON	When SYSPWR lower than setting,if VBUS voltage is enough, open VBUS rapidly.	R/W	1
7	VBUS_FST_OFF	When SYSPWR higher than setting, it will shut off VBUS rapidly.	R/W	1

6	WALL_FST_ON	When SYSPWR lower than setting,if WALL voltage is enough, open WALL rapidly.	R/W	1
5	WALL_FST_OFF	When SYSPWR higher than setting, it will shut off WALL rapidly.	R/W	1
4	BAT_FST_ON	When SYSPWR lower than setting,if BAT voltage is enough, open BAT rapidly.	R/W	1
3	BAT_FST_OFF	When SYSPWR higher than setting, it will shut off WALL rapidly.	R/W	1
2	VBUS_PD	VBUS 5K pull-down resistance enable	R/W	0
1	WALL_PD	WALL 5K pull-down resistance enable	R/W	0
0	Reserved	Reserved	R/W	0

11.4.61 AuxADC_CTL0

AuxADC_CTL0 Register （default 0xFFFF）

Offset = 0x3E

Bit(s)	Name	Description	R/W	Reset
15	AUXADC0_EN	AUXADC0 ADC enable 0: disable 1: enable	R/W	1
14	AUXADC1_EN	AUXADC1 ADC enable 0: disable 1: enable	R/W	1
13	AUXADC2_EN	AUXADC2 ADC enable 0: disable 1: enable	R/W	1
12	AUXADC3_EN	AUXADC3 ADC enable 0: disable 1: enable	R/W	1
11	VBUSVADC_EN	VBUS VOLATGE ADC enable 0: disable 1: enable	R/W	1
10	WALLVADC_EN	WALL VOLATGE ADC enable 0: disable 1: enable	R/W	1
9	SYSPWRADC_EN	SYSPWR VOLATGE ADC enable	R/W	1

		0: disable 1: enable		
8	BAKBATADC_EN	BAKBAT VOLTAGE ADC enable 0: disable 1: enable	R/W	1
7	BATVADC_EN	BAT VOLATGE ADC enable 0: disable 1: enable	R/W	1
6	TEMP_ADC	TEMP ADC enable 0: disable 1: enable	R/W	1
5	REMCON_ADC_EN	REMCON ADC enable 0: disable 1: enable	R/W	1
4	BATIADC_EN	BAT CURRENT ADC enable 0: disable 1: enable	R/W	1
3	WALLIADC_EN	WALL CURRENT ADC enable 0: disable 1: enable	R/W	1
2	VBUSIADC_EN	VBUS CURRENT ADC enable 0: disable 1: enable	R/W	1
1	CHGIADC_EN	Charger current ADC enable 0: disable 1: enable	R/W	1
0	IREFADC_EN/ SVCC_ADC_EN	CURRENT REF ADC enable/ SVCC ADC enable 0: disable 1: enable	R/W	1

11.4.62 AuxADC_CTL1

AuxADC_CTL1 Register （default 0x000B）

Offset = 0x3F

Bit(s)	Name	Description	R/W	Reset
15-4	Reserved	Reserved	R/W	0x0
3	ADC_COMP_TMEN	ADC COMP OFFSET TRIMMING	R/W	1

		0 : DISABLE 1 : ENABLE		
2	ADC_COMP_BIAS	ADC COMP BIAS 0: 4uA 1: 6uA	R/W	0
1	ADC_INPUT_RANGE	ADC INPUT RANGE 0: 0~1.5v 1: 0~3.0v	R/W	1
0	ADC_CLOCK_ADJ	ADC clock adjust 0: 300K 1: 400K	R/W	1

11.4.63 PMU_BATVADC

PMU_BATADC Register （default 0x0000）

Offset = 0x40

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0
9：0	BATVADC	BATVADC data	R	x

11.4.64 PMU_BATIADC

PMU_BATIADC Register （default 0x0000）

Offset = 0x41

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0
9：0	BATIADC	BATIADC data	R	x

11.4.65 PMU_WALLVADC

PMU_WALLADC Register （default 0x0000）

Offset = 0x42

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0

9：0	WALLVADC	WALLVADC data	R	x

11.4.66 PMU_WALLIADC

PMU_WALLIADC Register （default 0x0000）
Offset = 0x43

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0
9：0	WALLIADC	WALLIADC data	R	x

11.4.67 PMU_VBUSVADC

PMU_VBUSADC Register （default 0x0000）
Offset = 0x44

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0
9：0	VBUSVADC	VBUSVADC data	R	x

11.4.68 PMU_VBUSIADC

PMU_VBUSIADC Register （default 0x0000）
Offset = 0x45

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0
9：0	VBUSIADC	VBUSIADC data	R	x

11.4.69 PMU_SYSPWRADC

PMU_SYSPWRADC Register （default 0x0000）
Offset = 0x46

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0

9：0	SYSPWRADC	SYSPWRADC data	R	x

11.4.70 PMU_RemConADC

PMU_RemConADC Register （default 0x0000）
Offset = 0x47

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0
9：0	REMCONADC	REMCON ADC data	R	x

11.4.71 PMU_SVCCADC

PMU_SVCCADC Register （default 0x0000）
Offset = 0x48

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0
9：0	SVCCADC	SVCC ADC data	R	x

11.4.72 PMU_CHGIADC

PMU_ CHGIADC Register （default 0x0000）
Offset = 0x49

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0
9：0	CHGIADC	CHGIADC data	R	x

11.4.73 PMU_IREFADC

PMU_ IREFADC Register （default 0x0000）
Offset = 0x4A

Bit(s)	Name	Description	R/W	Reset

15-10	RESERVED	RESERVED	R	0
9：0	IREFADC	IREFADC data	R	x

11.4.74 PMU_BAKBATADC

PMU_ BAKBATADC Register （default 0x0000）
Offset = 0x4B

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0
9：0	BAKBATADC	BAK BATTERY VOLTAGE ADC data	R	x

11.4.75 PMU_ICTEMPADC

PMU_ ICTEMPADCRegister （default 0x0000）
Offset = 0x4C

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0
9：0	ICTEMPADC	ICTEMPADC ADC data	R	x

12. Auxiliaty ADC

12.1 Module Description

ATC260x contains 10-bit, 16-channel analog-to-digital converters (ADCs)， the purpose of each ADC distributes as follows:

ADC_0	ADC_1	ADC_2	ADC_3	ADC_4	ADC_5	ADC_6	ADC_7
BATv	BATI	VBUSV	VBUSI	SYSPWRV	WALLV	WALLI	ICHG
ADC_8	ADC_9	ADC_10	ADC_11	ADC_12	ADC_13	ADC_14	ADC_15
SVCC/ IREF	REM_ CON	ICTEMP	BAKBA T	AUXADC 0	AUXADC 1	AUXADC2	AUXAD C3

WALL、SYSPWR、VBUS will divided by 2.5 before sent to ADC，so the relation between voltage value of WALL、SYSPWR、VBUS and their ADC value is:

$$V = DATA * LSB * 2.5$$

While BAT will divided by 2 before sent to ADC, so the relation of BAT and its ADC is :

$$V = DATA * LSB * 2$$

In addition, ADC also needs to detect the current from VBUS to SYSPWR, from BAT to SYSPWR, charger's charging current, BAKE BAT voltage, SVCC voltage, battery tempreture and etc.

Among these, full scale range of BATI ADC and WALLI ADC、VBUSI ADC、ICHG is 1500mA，so the relation of their ADC data's corresponding current data is:

$$I = DATA * LSBI = DATA * 1500/1024(mA)$$

ICTEMP's ADC data and tempreture relationship is as follows:

$$TEMP = 0.1949 * DATA - 14.899(^{\circ}C)$$

For Remcon ADC，its input range is 0-3v，while drive-by-wire ADC is distinguished by button's different voltage. When the wire button's power voltage is changed, the corresponding voltage of same button is different, so Remcon ADC data reflects the ratio of Remcon voltage and SVCC voltage:

$$\mathrm{Re}\,mcon = (\mathrm{Re}\,mconADC\_DATA/1024) * SVCC$$

Among these， RemconADC_DATA/1024 could react different button's value, it shows the button's value is RemconADC_DATA/1024 times of SVCC 。

AUXADC0~3 is external general used ADC。

12.2 Register List

AUXADC Block Address

Name	Base Address
AUXADC	0x0000

Table 0-1 AUXADC Controller Registers

Offset	Register Name	Description
0x3E	AuxADC_CTL0	PMU AuxADC CONTROL Register0
0x3F	AuxADC_CTL1	PMU AuxADC CONTROL Register1
0x40	PMU_BATVADC	PMU BATVADC Register
0x41	PMU_BATIADC	PMU BATIADC Register
0x42	PMU_WALLVADC	PMU WALLVADC Register
0x43	PMU_WALLIADC	PMU WALLIADC Register
0x44	PMU_VBUSVADC	PMU VBUSVADC Register
0x45	PMU_VBUSIADC	PMU VBUSIADC Register
0x46	PMU_SYSPWRADC	PMU SYSPWRADC Register
0x47	PMU_RemConADC	PMU RemConADC Register
0x48	PMU_SVCCADC	PMU SVCCADC Register
0x49	PMU_CHGIADC	PMU CHGIADC Register
0x4A	PMU_IREFADC	PMU IREFADC Register
0x4B	PMU_BAKBATADC	PMU BAKBATADC Register
0x4C	PMU_ICTEMPADC	PMU ICTEMPADC Register
0x4D	AuxADC0	PMU AuxADC0 Register
0x4E	AuxADC1	PMU AuxADC1 Register
0x4F	AuxADC2	PMU AuxADC2 Register
0x50	AuxADC3	PMU AuxADC3 Register

12.2.1 AuxADC_CTL0

AuxADC_CTL0 Register （default 0xFFFF）

Offset = 0x3E

Bit(s)	Name	Description	R/W	Reset
15	AUXADC0_EN	AUXADC0 ADC enable 0: disable	R/W	1

		1: enable		
14	AUXADC1_EN	AUXADC1 ADC enable 0: disable 1: enable	R/W	1
13	AUXADC2_EN	AUXADC2 ADC enable 0: disable 1: enable	R/W	1
12	AUXADC3_EN	AUXADC3 ADC enable 0: disable 1: enable	R/W	1
11	VBUSVADC_EN	VBUS VOLATGE ADC enable 0: disable 1: enable	R/W	1
10	WALLVADC_EN	WALL VOLATGE ADC enable 0: disable 1: enable	R/W	1
9	SYSPWRADC_EN	SYSPWR VOLATGE ADC enable 0: disable 1: enable	R/W	1
8	BAKBATADC_EN	BAKBAT VOLTAGE ADC enable 0: disable 1: enable	R/W	1
7	BATVADC_EN	BAT VOLATGE ADC enable 0: disable 1: enable	R/W	1
6	TEMP_ADC	TEMP ADC enable 0: disable 1: enable	R/W	1
5	REMCON_ADC_EN	REMCON ADC enable 0: disable 1: enable	R/W	1
4	BATIADC_EN	BAT CURRENT ADC enable 0: disable 1: enable	R/W	1
3	WALLIADC_EN	WALL CURRENT ADC enable 0: disable 1: enable	R/W	1
2	VBUSIADC_EN	VBUS CURRENT ADC enable 0: disable 1: enable	R/W	1

1	CHGIADC_EN	Charger current ADC enable 0: disable 1: enable	R/W	1
0	IREFADC_EN/ SVCC_ADC_EN	CURRENT REF ADC enable/ SVCC ADC enable 0: disable 1: enable	R/W	1

12.2.2AuxADC_CTL1

AuxADC_CTL1 Register （default 0x000B）
Offset = 0x3F

Bit(s)	Name	Description	R/W	Reset
15-4	Reserved	Reserved	R/W	0x0
3	ADC_COMP_TMEN	ADC COMP OFFSET TRIMMING 0 : DISABLE 1 : ENABLE	R/W	1
2	ADC_COMP_BIAS	ADC COMP BIAS 0: 4uA 1: 6uA	R/W	0
1	ADC_INPUT_RANGE	ADC INPUT RANGE 0: 0~1.5v 1: 0~3.0v	R/W	1
0	ADC_CLOCK_ADJ	ADC clock adjust 0: 300K 1: 400K	R/W	1

12.2.3 AuxADC_BATV

BATADC Register （default 0x0000）
Offset = 0x40

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0
9：0	BATVADC	BATVADC data	R	x

12.2.4 AuxADC_BATI

BATIADC Register （default 0x0000）
Offset = 0x41

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0
9：0	BATIADC	BATIADC data	R	x

12.2.5 AuxADC_WALLV

WALLADC Register （default 0x0000）
Offset = 0x42

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0
9：0	WALLVADC	WALLVADC data	R	x

12.2.6 AuxADC__WALLI

WALLIADC Register （default 0x0000）
Offset = 0x43

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0
9：0	WALLIADC	WALLIADC data	R	x

12.2.7 AuxADC__VBUSV

VBUSADC Register （default 0x0000）
Offset = 0x44

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0
9：0	VBUSVADC	VBUSVADC data	R	x

12.2.8 AuxADC_VBUSI

VBUSIADC Register （default 0x0000）
Offset = 0x45

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0
9：0	VBUSIADC	VBUSIADC data	R	x

12.2.9 AuxADC_SYSPWR

SYSPWRADC Register （default 0x0000）
Offset = 0x46

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0
9：0	SYSPWRADC	SYSPWRADC data	R	x

12.2.10 AuxADC_RemCon

RemConADC Register （default 0x0000）
Offset = 0x47

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0
9：0	REMCONADC	REMCON ADC data	R	x

12.2.11 AuxADC_SVCC

SVCCADC Register （default 0x0000）
Offset = 0x48

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0
9：0	SVCCADC	SVCC ADC data	R	x

12.2.12 AuxADC_CHGI

CHGIADC Register （default 0x0000）
Offset = 0x49

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0
9：0	CHGIADC	CHGIADC data	R	x

12.2.13 AuxADC_IREF

IREFADC Register （default 0x0000）
Offset = 0x4A

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0
9：0	IREFADC	IREFADC data	R	x

12.2.14 AuxADC_BAKBAT

BAKBATADC Register （default 0x0000）
Offset = 0x4B

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0
9：0	BAKBATADC	BAK BATTERY VOLTAGE ADC data	R	x

12.2.15 AuxADC_ICTEMP

ICTEMPADCRegister （default 0x0000）
Offset = 0x4C

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0
9：0	ICTEMPADC	ICTEMPADC ADC data	R	x

12.2.16 AuxADC0

AuxADC0 Register （default 0x0000）
Offset = 0x4D

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0
9：0	AuxADC0	AuxADC0 data	R	x

12.2.17 AuxADC1

PMU_ AuxADC1 Register （default 0x0000）
Offset = 0x4E

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0
9：0	AUXADC1	AUXADC1 data	R	x

12.2.18 AuxADC2

PMU_ AuxADC2 Register （default 0x0000）
Offset = 0x4F

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0
9：0	AUXADC2	AUXADC2 data	R	x

12.2.19 AuxADC3

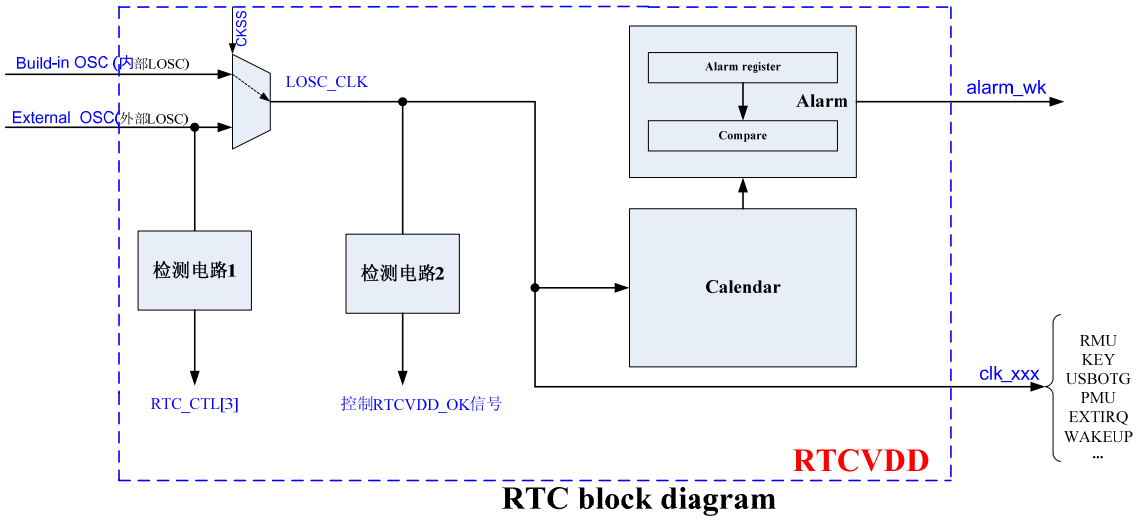
PMU_ AuxADC3 Register （default 0x0000）
Offset = 0x50

Bit(s)	Name	Description	R/W	Reset
15-10	RESERVED	RESERVED	R	0
9：0	AUXADC3	AUXADC3 data	R	x

13. Real-Time Clock

13.1 Module Description

RTC module is used in timing and alarm clock etc function, it supports power off alarm clock and timing power on.

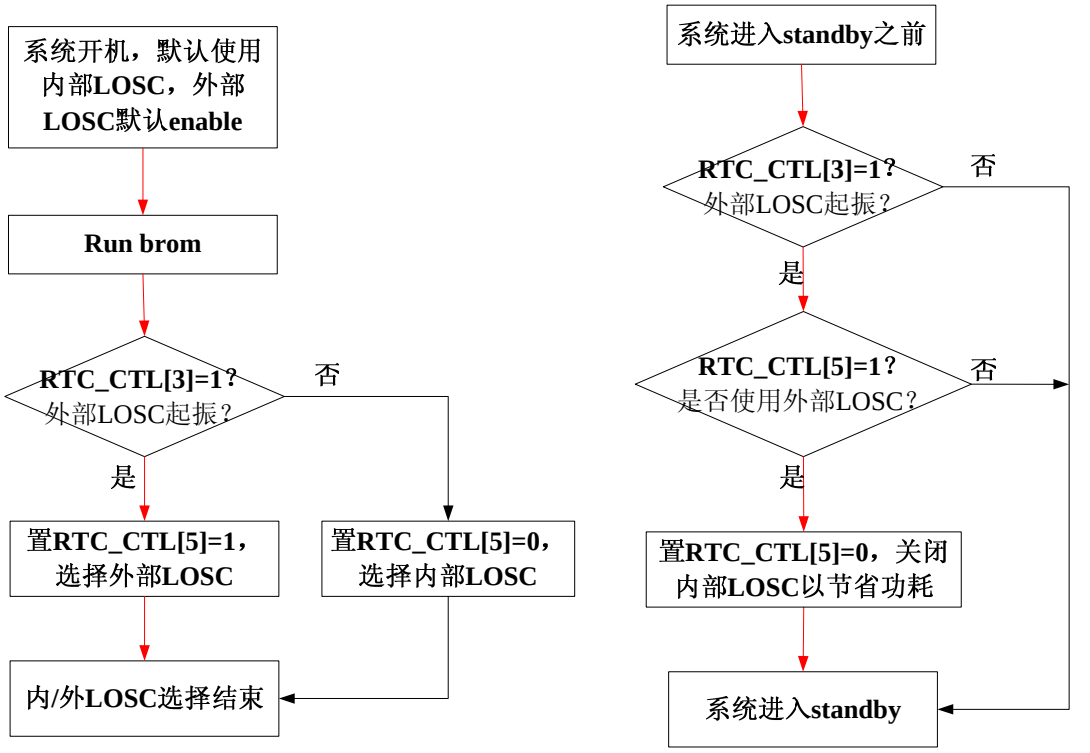


RTC block diagram

Figure 0-1

External LOSC detects working circuit's sequence: if it detects that LOSC has oscillationwave, then detecting circuit 1 will delay about 1ms to configure register RTC_CTL[3] as 1. If detecting the external LOSC has no oscillationwave, then detecting circuit 1 will delay about 3ms to configure register RTC_CTL[3] as 0. Detecting circuit 2 has the same function with this, if the system use LOSC_CLK and there is no clock, then RTCVDD_OK's signal will be pulled down, and the whole system reseted.

When the system power on and enter to standby, its inner/outer LOSC manage process is(red arrow is LOSC's external normal flow):



开机时内/外LOSC的切换流程　　进入standby之前的内/外LOSC处理流程

Figure 0-2

The handle of external LOSC oscillation stop: no matter the system is standby or in normal running mode, only if system chooses the external LOSC and the external is stop oscillation, detecting circuit 2 will pull down RTCVDD_OK signal, the whole system reset. Then you power on, system default use internal LOSC, it can run well as the above flow.

Calendar

When *RTCE*=1, ***RTC_H***、***RTC_MS*** and ***RTC_YMD*** count up with LOSC_CLK. CPU can read the two registers at any time for getting the real time, but can not write the two registers. When *RTCE*=0, the two registers can be written to set the real time.

Alarm

when RTCE=ALIE=1,if RTC_HALM=RTC_H、RTC_MSALM=RTC_MS and ***RTC_YMDALM=RTC_YMD***, Alarm IRQ will generate,It can be cleared by writing 1 to the bit *ALIP*.

13.2 Register List

RTC Block Address

Name	Base Address
RTC	0x0000

Table 0-1 **RTC Controller Registers**

Offset	Register Name	Description
0x52	RTC_CTL	RTC control register
0x53	RTC_MSALM	RTC ALARM Minute second REGISER
0x54	RTC_HALM	RTC ALARM Hour REGISER
0x55	RTC_YMDALM	RTC ALARM Year month date REGISER
0x56	RTC_MS	RTC Minute second REGISER
0x57	RTC_H	RTC Hour REGISER
0x58	RTC_DC	RTC day century REGISER
0x59	RTC_YMD	RTC year month date REGISER

13.2.1 RTC_CTL

Calendar Control Register （default 0x5A50）

Offset=0x052

Bits	Name	Description	Access	Reset
15:14	LGS	Low frequency crystal Oscillator GMNIN select bits 00： 01： 10： 11：	R/W	01
13：12	LOSC_CP	LOSC Capacitor Select： 00：12pF 01：15pF 10：18pF 11：21pF	R/W	01
11	RST	RTC Reset 1: Normal 0: Reset	R/W	1

10	VERI	Rtc Verify Clock Enable Switch RTC clock to 32k 1: Enable 0: Disable	R/W	0
9	LEAP	RTC Leap Year bit 1: leap year 0: not leap year	R	1
8:7	TEST	In test mode, select 4 test clock out to RTC test pad 0：2Hz 1：8Hz 2：128Hz 3：32KHz	R/W	0
6	EOSC	External Crystal OSC enable 1: Enable 0: Disable	R/W	1
5	CKSS0	RTC_32K clock Source Select 1: External Crystal OSC 0: Build-in OSC	R/W	0
4	RTCE	RTC Enable 1: Enable 0: Disable	R/W	1
3	Ext_LOSC_State	External LOSC State： 0：external LOSC stop Oscillating 1：external LOSC is Oscillating	R	X
2	-	Reserved	R	0
1	ALIE	Alarm IRQ Enable 1: Enable 0: Dsiable	R/W	0
0	ALIP	Alarm IRQ Pending bit, writing 1 to this bit will clear it	R/W	0

Note ：

1、 bit5: only when RTCVDD power off thorough, CKSS0 will be reseted.

2、Calendar and Alarm mode need accurate low frequency CLK, so choose the accurate External Crystal OSC in application.

3、LOSC_CP[15:14]：the match capacitance of LOSC circuit choosing. It all depends on external 32.768KHz crystal load capacitance, the default step is usually 01 or 10.

4、LGS[13:12]：the drive capacity strength of LOSC circuit, the sequence of drive ability is 2b11>2b10>2b01>2b00，default is recommend used.

5、TEST[8:7]：Debug back door of LOSC.

6、CKSS0[5]：external LOSC and IC internal LOSC choose to change bit.

7、Ext_LOSC_State[3]：external LOSC oscillation state bit.

13.2.2 RTC_MSALM

Calendar MSALM Register （default 0x0000）
Offset=0x053

Bits	Name	Description	Access	Reset
15:12	-	Reserved	R	0
11:6	MINAL	Alarm minute setting 00H – 3BH	R/W	0
5:0	SECAL	Alarm second setting 00H – 3BH	R/W	0

13.2.3 RTC_HALM

Calendar HALM Register （default 0x0000）
Offset=0x054

Bits	Name	Description	Access	Reset
15:5	-	Reserved	R	0
4:0	HOUEAL	Alarm hour setting 00H – 17H	R/W	0

13.2.4 RTC _YMDALM

Calendar YMDALM Register （default 0x0000）
Offset=0x055

Bits	Name	Description	Access	Reset
15:9	YEARAL	Alarm year setting 00H – 63H	R/W	0
8:5	MONAL	Alarm month setting 01H – 0CH	R/W	0
4:0	DATEAL	Alarm day setting 01H – 1FH	R/W	0

13.2.5 RTC_MS

Calendar MS Register （default 0x0000）
Offset=0x056

Bits	Name	Description	Access	Reset
15:12	-	Reserved	R	0
11:6	MIN	Time minute setting 00H – 3BH	R/W	0
5:0	SEC	Time second setting 00H – 3BH	R/W	0

13.2.6 RTC_H

Calendar HOUR Register （default 0x0000）
Offset=0x057

Bits	Name	Description	Access	Reset
15:5	-	Reserved	R	0
4:0	HOUR	Time hour setting 00H – 17H	R/W	0

13.2.7 RTC_DC

Calendar DC Register （default 0x0080）
Offset=0x058

Bits	Name	Description	Access	Reset
15:10	-	Reserved	R	0
9:7	DAY	Time day setting 01H – 07H	R/W	001
6:0	CENT	Time setting 00H – 63H	R/W	0

13.2.8 RTC_YMD

Calendar YMD Register （default 0x0021）

Offset=0x059

Bits	Name	Description	Access	Reset
15:9	YEAR	Time year setting 00H – 63H	R/W	0
8:5	MON	Time month setting 01H – 0CH	R/W	0001
4:0	DATE	Time day setting 01H – 1FH	R/W	00001

14. Infrared Remote Controller

14.1 Features

Support RC5\9012\NEC(8bit)\AIR protocol, compatible 36kHz, 38kHz, 40kHz carrier.
Support IRC wake up
Need to connect an IR receiver when use.
IRC module would generate the wake up signal to PMU only when the received key data equal to the IRC_WK register ‘s data，include NEC、9012、RC5 and AIR mode.

Support RC5\9012\NEC(8bit)\AIR protocol, compatible 36kHz, 38kHz, 40kHz carrier.
Support IRC wake up
Need to connect an IR receiver when use.
IRC module would generate the wake up signal to PMU only when the received key data equal to the IRC_WK register ‘s data，include NEC、9012、RC5 and AIR mode.

14.2Features Module Description

9012 Protocol

The 9012 protocol uses a pulse distance encoding of the bits. Each pulse is one Tm (560μs) long 38kHz carrier burst. A logical "1" takes 4Tm (2.25ms) to transmit, while a logical "0" is only 2Tm (1.12ms). The recommended carrier duty-cycle is 1/4 or 1/3.

Tm=256/Fosc=0.56ms (Fosc=455kHz)
Repetition time=192Tm=108ms
Carrier frequency = Fosc/12
8 bit customer code and 8 bit command code length
customer and command are transmitted twice for reliability
Pulse distance modulation
Bit time of 2Tm(1.12ms) for logic “0” or 4Tm (2.25ms) for logic “1”
With this protocol the LSB is transmitted first. In this case Customer code and Command is transmitted. A message is started by 8Tm (4.5ms) AGC burst, which was used to set the gain of the earlier IR receivers. This AGC burst is then followed by 8Tm (4.5ms) space, which is then followed by the Customer code and Command. Customer code and Command are transmitted twice. The second

time the command bits are inverted and can be used for verification of the received message.

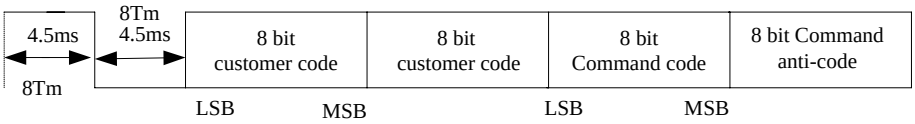


Figure 0-1

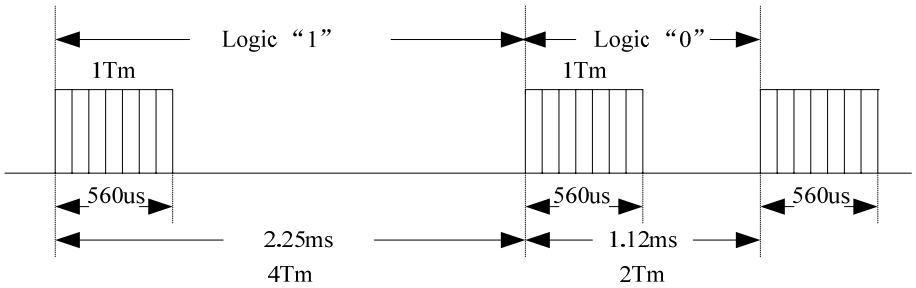


Figure 0-2

A command is transmitted only once, even when the key on the remote control remains pressed. Every 192Tm a repeat code is transmitted for as long as the key remains down. This repeat code is simply one 8Tm (4.5ms) AGC pulse followed by one 8Tm (4.5ms) space and a logic “1” +1Tm (560µs) burst.

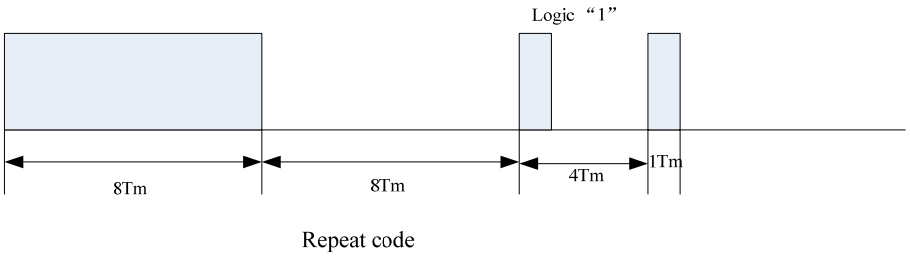


Figure 0-3

NEC Protocol(8bit)

The NEC protocol uses a pulse distance encoding of the bits. Each pulse is one Tm (560µs) long 38kHz carrier burst. A logical "1" takes 4Tm (2.25ms) to transmit, while a logical "0" is only 2Tm (1.12ms). The recommended carrier duty-cycle is 1/4 or 1/3.

Tm=256/Fosc=0.56ms (Fosc=455kHz)
Repetition time=192Tm=108ms
Carrier frequency = Fosc/12
8 bit customer and 8 bit command length

customer and command are transmitted twice for reliability

Pulse distance modulation

Bit time of 2Tm(1.12ms) for logic “0” or 4Tm (2.25ms) for logic “1”

With this protocol the LSB is transmitted first. In this case Customer code and Command is transmitted. A message is started by 16Tm (9ms) AGC burst, which was used to set the gain of the earlier IR receivers. This AGC burst is then followed by 8Tm (4.5ms) space, which is then followed by the Customer code and Command. Customer code and Command are transmitted twice. The second time all bits are inverted and can be used for verification of the received message. The total transmission time is constant because every bit is repeated with its inverted length.

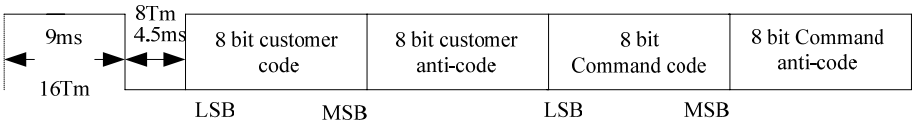


Figure 0-4

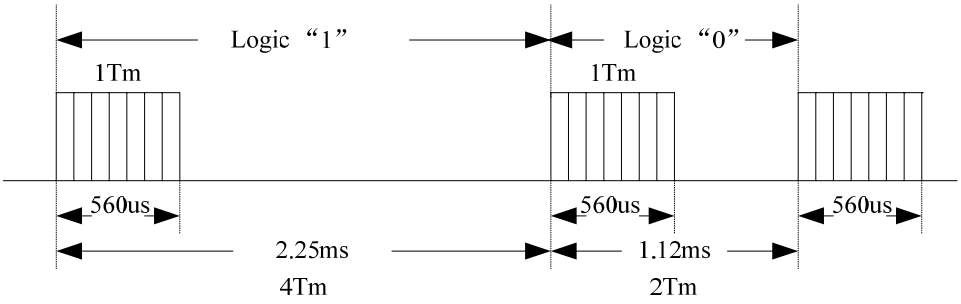


Figure 0-5

A command is transmitted only once, even when the key on the remote control remains pressed. Every 192Tm a repeat code is transmitted for as long as the key remains down. This repeat code is simply a 16Tm (9ms) AGC pulse followed by a 4Tm (2.25ms) space and one Tm (560µs) burst.

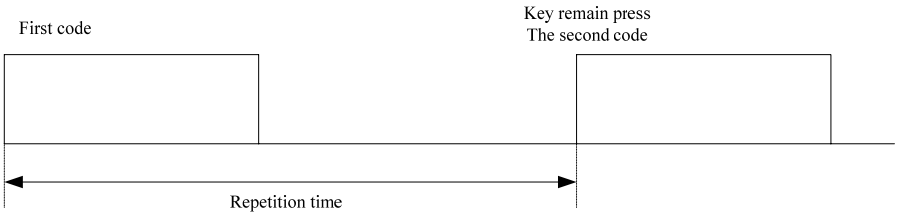
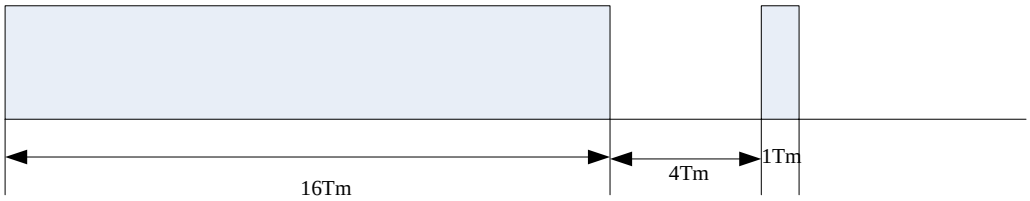


Figure 0-6



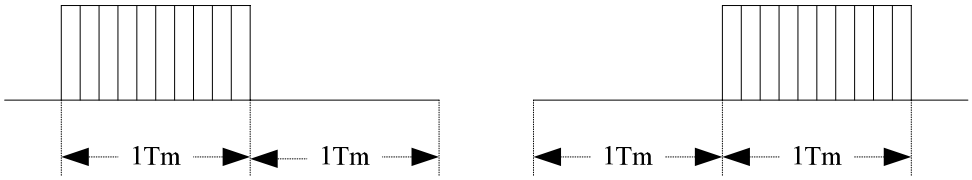
Repeat code

Figure 0-7

RC5 Protocol

The protocol uses bi-phase modulation (or so-called Manchester coding) of a 38kHz IR carrier frequency. All bits are of equal length of 1.8ms in this protocol, with half of the bit time filled with a burst of the 38kHz carrier and the other half being idle. A logical zero is represented by a burst in the first half of the bit time. A logical one is represented by a burst in the second half of the bit time. The pulse/pause ratio of the 38kHz carrier frequency is 1/3 or 1/4, to reduce power consumption.

1 bit-time = 3 x 256 /Fosc= 1.688ms (Fosc=455kHz)
Tm= 1 bit-time/2=0.844ms
Repetition time= 4 x 16 x 2Tm=108ms
Carrier frequency = Fosc/12



Logic 0 Logic 1

Figure 0-8

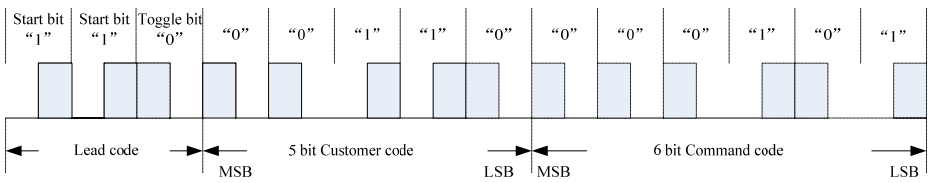


Figure 0-9

The first two pulses are the start pulses, and are both logical "1". Please note that half a bit time is elapsed before the receiver will notice the real start of the message.
The 3d bit is a toggle bit. This bit is inverted every time a key is released and pressed again. This way the receiver can distinguish between a key that remains down, or is pressed repeatedly.
The next 5 bits represent the IR device address, which is sent with MSB first. The address is followed by a 6 bit command, again sent with MSB first.
A message consists of a total of 14 bits, which adds up to a total duration of 28Tm. Sometimes a message may appear to be shorter because the first half of the start bit S1 remains idle. And if the last bit of the message is a logic "0" the last half bit of the message is idle too.
As long as a key remains down the message will be repeated every 128Tm(108ms). The toggle bit will retain the same logical level during all of these repeated messages. It is up to the receiver software to interpret this auto repeat feature.

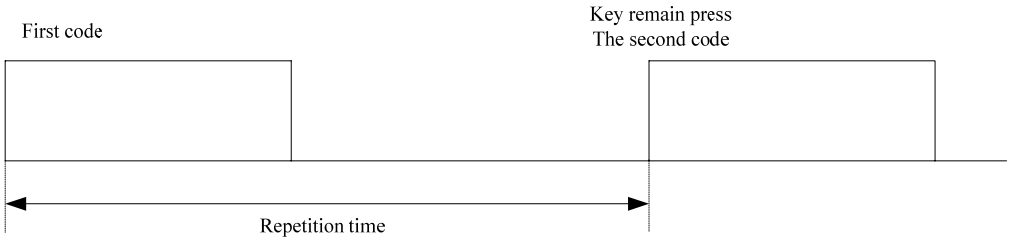


Figure 0-10

AIR Protocol

The AIR protocol uses a pulse distance encoding of the bits. The recommended carrier duty-cycle is 1/3.
Logic Bit：

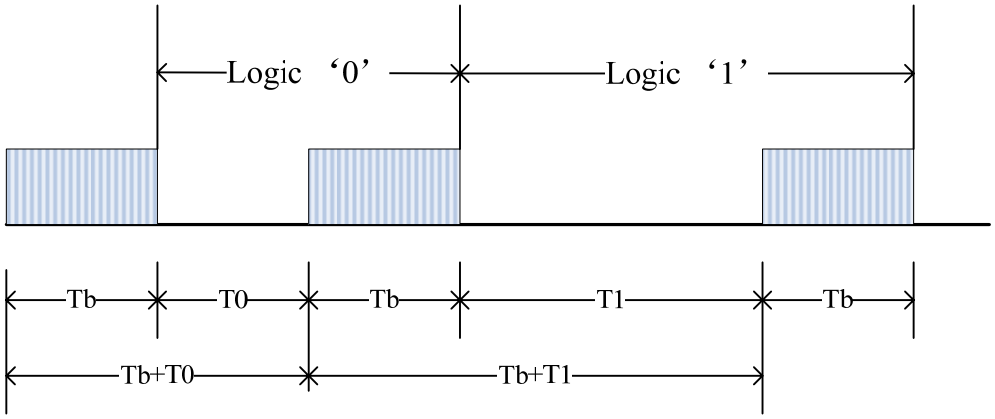


Figure 0-11

Tb = 190us ≌ 6 D_T ; T0 = Tb = 190us； T1 = 360us;

Start Symbol：

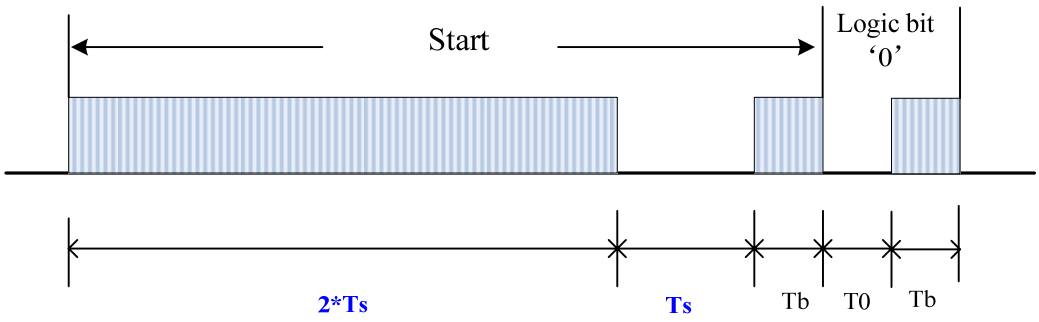


Figure 0-12

Ts = 500us, Start Symbol: Ts+2*Ts+Tb =1690us。

Frame:

One start symbol and 18-bit data compose the Frame. ADDR, T0, KEY 0, T1, KEY 1，CHKSUM compose the 18-bit data.

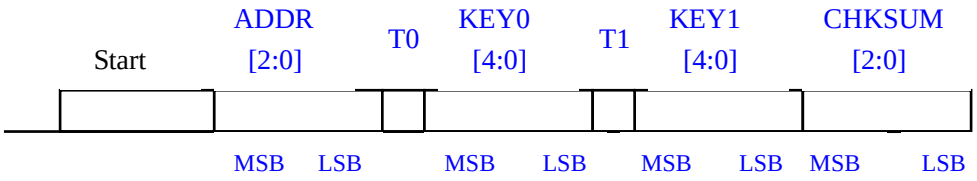


Figure 0-13

Name	Attribute	Purpose
Start	1 Start Symbol	Detect Frame、AGC、Clock synchronize
ADDR	3 Normal Bit	Customer code
T0	1 Normal Bit	Toggle bit 0
KEY 0	5 Normal Bit	Key Index 0
T1	1 Normal Bit	Toggle bit 1
KEY 1	5 Normal Bit	Key Index 1
CHKSUM	3 Normal Bit	Check bit

Notes：except the Start is Start Symbol， the other all is Normal data bit。

KEY 0/KEY 1： each support 31 keys, and the data b’00000 indicate that no key pressed down.

Toggle bit（T0/T1）： Toggle bit change when the key 0 or key 1 is press down and release between the two sequence frame. The Toggle bit not change for as long as the key remains down.

Checksum: 3bit， check the receive data

Checksum[2:0] = { Address[2:0] } xor { T0, Key0[4:3] } xor { Key0[2:0] }
xor {T1, Key1[4:3]} xor { Key1[2:0] };

Repeat interval:

When the key is remain pressed down, the repeat code as below:

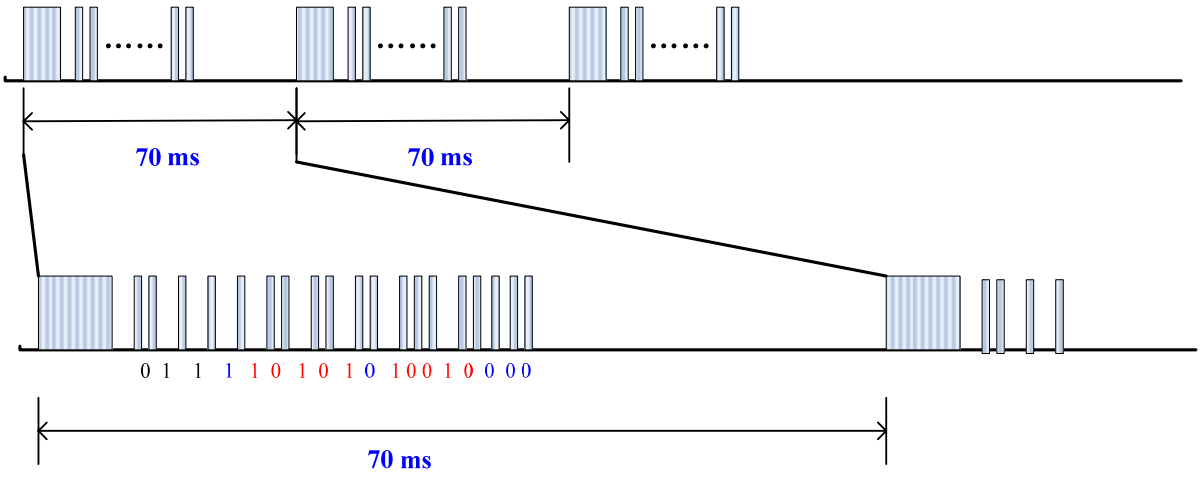


Figure 0-14

14.3 Register List

IRC Block Address

Name	Base Address
IRC	0x0000

Table 0-1 **IRC Controller Registers**

Offset	Register Name	Description
0x60	IRC_CTL	Infrared remote control register
0x61	IRC_STAT	Infrared remote status register
0x62	IRC_CC	Infrared remote control customer code register
0x63	IRC_KDC	Infrared remote control KEY

		data code register
0x64	IRC_WK	Infrared remote control wake up KEY data code register

14.3.1 IRC_CTL

Infrared remote control register （default 0x0000）
Offset = 0x60

Bit(s)	Name	Description	R/W	Reset
15:4	Reserved	Reserved	R	0x0
3	IRE	IRC enable 0: disable 1: enable	RW	0x0
2	IIE	IRC IRQ enable 0: disable 1:enable	RW	0x0
1:0	ICMS	IRC code mode select 00: 9012 code 01: 8bits NEC code 10: RC5 code 11: AIR code	RW	0x0

14.3.2 IRC_STAT

Infrared remote control register （default 0x0000）
Offset = 0x61

Bit(s)	Name	Description	R/W	Reset
15:7	Reserved	Reserved	R	0x0
6	UCMP	User code don’t match pending bit. Write 1 to this bit will clear it, or auto clear if receive the correct user code the next time. 0: user code match 1: user code don’t match	RW	0x0
5	KDCM	Key data code don’t match pending bit. Write 1 to this bit will clear it, or auto clear if receive the	RW	0x0

		correct key data code the next time 0: key data code match 1: key data code don't match		
4	RCD	Repeated code detected, write 1 to this bit will clear it, otherwise don't change 0: no repeat code 1: detect repeat code	RW	0
3	-	Reserved	R	0x0
2	IIP	IRC IRQ pending bit, write 1 to this bit will clear it 0: no IRQ pending 1: IRQ pending The condition of suspending is that receiving all code correctly. It contains user code and key assignment,received correctly. And if user code and key assignment can received incorrectly, the receiving repeat code which followed this frame cannot happen to suspend.	RW	0x0
1	-	Reserved	R	0x0
0	IREP	IRC receive error pending 0: receive ok 1: receive error occurs if not match the protocol. Writing 1 to this bit will clear this bit, or auto clear if receive the correct user code and key data code the next time.	RW	0x0

14.3.3 IRC_CC

Infrared remote control customer code register （default 0x0000）

Offset = 0x62

Bit(s)	Name	Description	R/W	Reset
15:0	ICCC	Infrared remote control customer code In RC5 mode: Bit 4:0 is the customer code In 9012 and NEC mode: Bit 15:0 is the customer code, In AIR mode:	RW	0x0

		Bit2:0 is the address If the received customer code not comply with this register value, error occur.		

14.3.4 IRC_KDC

Infrared remote control KEY data code register （default 0x0000）
Offset = 0x63

Bit(s)	Name	Description	R/W	Reset
15:0	IKDC	IRC key data code In RC5 mode: Bit 5:0 is the Key data In 9012 and NEC mode: Bit 7:0 is the Key data; Bit 15:8 is the Key anti-data In AIR mode: Bit13 is the toggle bit Bit12:8 is the key1 data Bit5 is the toggle bit Bit 4:0 is the key0 data. If receiving key assignment, register should be update; if receiving repeat code, then register should not update.	RW	0x0

14.3.5 IRC_WK

Infrared remote control wake up KEY data code register （default 0x0000）
Offset = 0x64

Bit(s)	Name	Description	R/W	Reset
15:0	IKDC	IRC wake up key data code In RC5 mode: Bit 5:0 is the wake up Key data In 9012 and NEC mode: Bit15:0 is the wake up key data; Bit 7:0 is the Key data; Bit 15:8 is the Key anti-data In AIR mode:	RW	0x0

		Bit 4:0 is the wake up key data (use key0 data). If the receiving key assignment is the same as the value of register, then it will generate wakeup signal to PMU mode, and suspending at the same time.		

15. Ethernet PHY Subsystem

15.1Features

RMII interface support with 50MHz reference clock output to MAC
SMII interface support with 125MHz reference clock output to MAC
Not supports SMI interface access the PHY register directly, the PHY register accessed by SPI interface
Single-chip 10Base-T and 100Base-TX physical layer solution
Fully compliant to 100BASE-TX/10BASE-T standards (IEEE 802.3u, FDDI-TP-PMD, and IEEE 802.3)
Supports two multi-functional LED output
Supports the full-duplex and half-duplex modes
Supports Auto-MDIX for detection and correction with the MDI/MDIX auto-crossover function

15.2 Function Description

- This PHY integrated 10/100BASE-TX (Twisted-pair cable) transceiver module achieves the high performance that can be realized in a wide variety of Ethernet applications. It is fully compliant with the 10/100BASE-TX Ethernet standards, such as IEEE 802.3, 802.3u, and ANSI X3.263-1995 (FDDI-TP-PMD).
- This PHY offers a choice of RMII or SMII data interface connection with the MAC processor. The MII Serial management bus (SMI) of MAC can not access to this PHY's control and status registers. User can use the SPI interface to configure the SMI control block of this PHY to access the PHY's internal control and status registers.
- This PHY does not require a 50MHz and 125MHz system clock. It uses a 24MHz or 25MHz crystal for its input reference clock and outputs a 50MHz RMII or 125MHz SMII reference clock to the MAC.
- The transmit and Receive function converts the received/transmitted data based on the IEEE 802.3 defined coding standards, such as the parallel-to-serial conversion, 4B/5B,scrambling/de-scrambling, NRZ-to-NRZI conversion and MLT3 encoding/decoding.

16. Touch Pannel

16.1 Features

Support 4 wire resistance touch panel
12 bit ADC resolution,single piont only.
X and Y direction's measurement independently
Sample Frequency from 1/4K~32K
Can be configed as 2-channel ADC when touch panel's function is not required
Support touch pressure measurement

16.2 Function Description

ATC260X integrates an 12 bit SAR ADC for Touch panel or 2-channel ADC. When enabled, the ADC will work.

When TEN and TIE set, the controller waits for touch and IRQ occurs while touched. Voltage of Y2 pulled low will trigger touch. After IRQ, software should set XYDS to enable X or Y direction's measurement and ADC conversion. Otherwise the SAR ADC would not work. The block will sample the voltage of X1 or Y1 and convert the analog voltage to digital bits through SAR ADC. The ADC data is available when YDR/XDR is set. The convert state described as below:

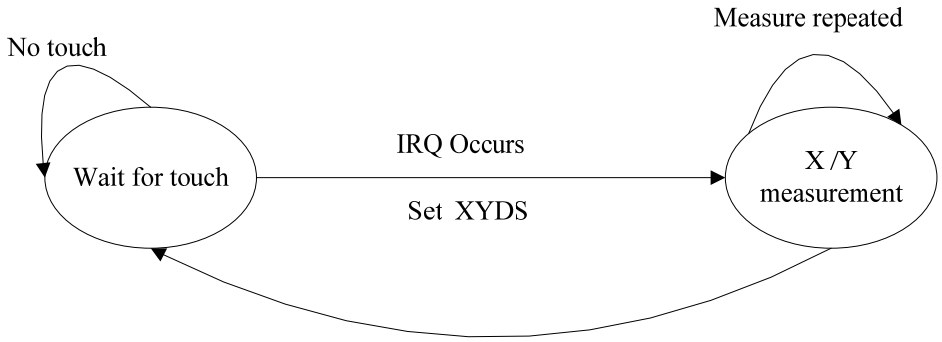


Figure 2.1-1

The SAR ADC's frequency (FSS) can be set between 1/2K~32K. Sampling time duty (STD) can be set as 1/8 or 1/16.These parameters are adjustable in demand. The timing described as below:

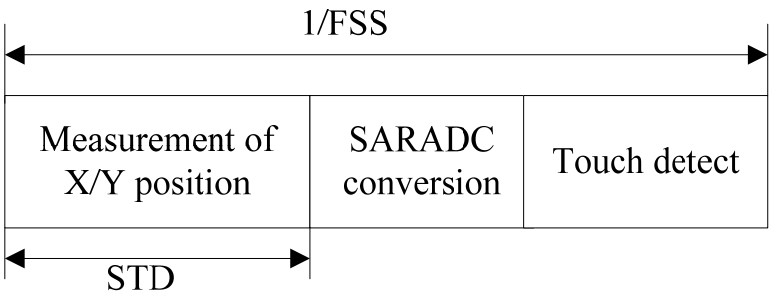


Figure 2.1-2

SAR ADC can be enabled by TEN or LEN or REN. When Touch panel's function is not required, this module can also be used as a 2-channel ADC. Touch panel and 2-channel ADC must not be used at the same time. LEN and REN can be set alone or together.
Touch panel and 2-channel ADC share the same control and data register. The data register is common. The bits of control allocated list below.
Common bits :
ADCBCS, STD, DFEN
Exclusive bits for touch panel:
TEN, XYDS, IDLE, NOTCH, TIE, TIP XDR, YDR
Exclusive bits for 2-channel ADC:
LEN, REN, LCIE, RCIE, LCIP, RCIP

When touch panel's function is selected, the bits distributed to 2-channel ADC must not be set, vice versa.
The voltage range of TP can be adjusted by setting register. VHLST of TP_CTL0 selects the V-pp of TP. The higher voltage may increase SNR of TP, but more power consummation will be taken.
Touch panel can also be used for waking up system. There are 1 mode function : Touch panel can wakeup PMU.
X1/X2/Y1/Y2 share pins with GPIO either.

16.3 Touch Pressure Measurement

The resistant of touch reflects the touch pressure. So the touch pressure measurement is identified to measure R_{touch}. The bigger of R_{touch}, the less of touch pressure, vice versa.

16.4 Register List

内容？

16.5 Register Description

内容？

17. Interrupt Controller

17.1 Features

16 Interrupt Sources can be send to INTC module of Master SOC through pin EXTIRQ . Table 0-1 shows all interrupt sources. Details about the interrupt sources can be found in the respective module sections.

Table 0-2 Interrupt Sources list

Interrupt Number	Sources	Type
0	AUDIO	High Level
1	TP	High Level
2	Ethernet	High Level
3	OV	High Level
4	OC	High Level
5	OT	High Level
6	UV	High Level
7	ALARM	High Level
8	Onoff	High Level
9	WKUP	High Level
10	IR	High Level
11-15	Reserved	-

Note: OV-over voltage, OC-over current, OT-over temperature, UV- Under-voltage.

If you want to know which interrupt has happened, please refer to register INTS_PD, you can mask any of the 16 interrupt sources by setting register INTS_MSK.

17.2 Block Diagram

The block diagram is as follows:

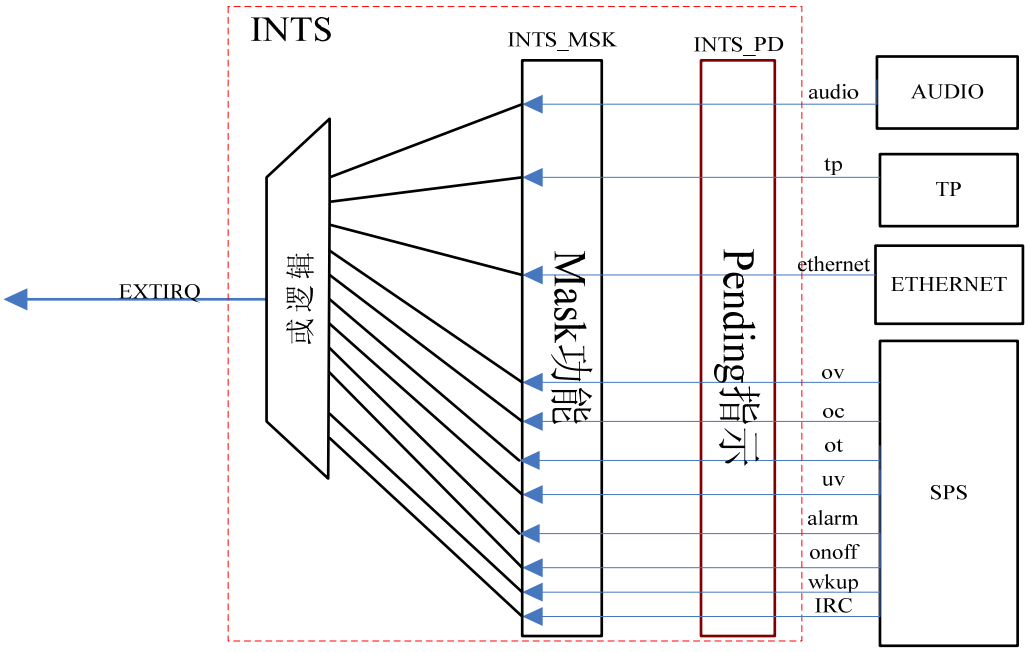


Figure 0-1

17.3 Register List

Interrupt source Block Base Address

Name	Base Address
INTS_Register	0x200

Interrupt source Block Configuration Registers List

Offset	Register Name	Description
0x00	INTS_PD	Interrupt Pending register
0x01	INTS_MSK	Interrupt Mask register

17.4 Register Description

17.4.1 INTS_PD

CPU can access the status of interrupt sources by read this register. Interrupt Pending bit can not be cleared by writing 1,it is not cleared until device pending is cleared.

offset = 0x00

Bit	Name	Description	R/W	Reset
15:11		Reserved		
10:0	INTS_PD[n]	Interrupt Pending bit. Interrupt name "n" accords to **Interrupt Sources Table.** 0: Interrupt source n request is not active 1: Interrupt source n request is active.	R	INTS_PD[n]

17.4.2 INTS_MSK

CPU can enable or disable by write this register. 0: Interrupt is disabled. 1: Interrupt is enabled.

offset = 0x01

Bits	Name	Description	R/W	Reset
15:11	Reserved	-	R/W	0
10	IR	IR Intterupt Mask Bit	R/W	0
9	WKUP	WKUP Interrupt Mask Bit	R/W	0
8	Onoff	Onoff Interrupt Mask Bit	R/W	0
7	ALARM	ALARM Interrupt Mask Bit	R/W	0
6	UV	UN-VOLTAGE Interrupt Mask Bit	R/W	0
5	OT	OVER TEMPERATURE Interrupt Mask Bit	R/W	0
4	OC	OVER CURRENT Interrupt Mask Bit	R/W	0
3	OV	OVER VOLTAGE Interrupt Mask Bit	R/W	0
2	Ethernet	Ethernet Interrupt Mask Bit	R/W	0
1	TP	TOUCH PANEL Interrupt Mask Bit	R/W	0
0	AUDIO	AUDIO Interrupt Mask Bit	R/W	0

18. General Puppose I/O

18.1 Features

This chapter will describe the multiplexing of the whole system and the GPIO function. There are 32 bits General purpose I/O port in ATC260X to bring more flexible application possibility. The multiplexing is software controlled and can be configured for different application.

18.2 Function Description

32 GPIOs with independent output and input function
Several different driving capacity of GPIOs
Software control for Multiplexing

18.3 Registers List

GPIO/MFP Registers Block base Address

Name	Base Address
MFP_Register	0x300

GPIO/MFP Registers Offset Address

Offset	Register Name	Description
0x00	MFP_CTL0	Multiplexing Control 0
0x01	MFP_CTL1	Multiplexing Control 1
0x10	GPIO_OUTEN0	GPIO Output Enable 0
0x11	GPIO_OUTEN1	GPIO Output Enable 1
0x12	GPIO_INEN0	GPIO Input Enable 0
0x13	GPIO_INEN1	GPIO Input Enable 1
0x14	GPIO_DAT0	GPIO Data 0
0x15	GPIO_DAT1	GPIO Data 1
0x20	PAD_DRV0	PAD Drive Capacity0 Select
0x21	PAD_DRV1	PAD Drive Capacity1 Select
0x22	PAD_EN	PAD enable control

18.4 Register Description

18.4.1 MFP_CTL0

Multiplexing Control Register 0
Offset=0x00

Bits	Name	Description	R/W	Default
15:8	-	Reserved	R	0
7	LED1	LED1 Multiplexing 0: LED1 1: GPIO29	RW	0
6	LED0	LED0 Multiplexing 0: LED0 1: GPIO28	RW	0
5	I2S_MCLK1_LRCLK1_DOUT	I2S_MCLK1、I2S_LRCLK1、I2S_DOUT Multiplexing 0: I2S_MCLK1 、 I2S_LRCLK1 and I2S_DOUT 1: GPIO9、GPIO10 and GPIO11	RW	0
4	I2S_MCLK0_LRCLK0	I2S_MCLK0 and I2S_LRCLK0 Multiplexing 0: I2S_MCLK0 and I2S_LRCLK0 1: GPIO6 and GPIO7	RW	0
3:2	I2S_DIN	I2S_DIN Multiplexing 00: I2S_DIN 01: GPIO8 10: I2S_DOUT 11:Reserved	RW	00
1:0	RMII	RMII Multiplexing 00: RMII_REF_CLK、RMII_CRS_DV、RMII_RXD0 、 RMII_RXD1 、 RMII_TX_EN 、 RMII_TXD0 and RMII_TXD1 01: GPIO21→ GPIO27 10: SMII_CLK、 SMII_RX、GPIO23→ GPIO25、SMII_TX and SMII_SYNC 11: Reserved	RW	00

18.4.2 MFP_CTL1

Multiplexing Control Register 1
Offset=0x01

Bits	Name	Description	R/W	Default
15:14	OUTSWC	OUTSWC Multiplexing 00: OUTSW and OUTC 01: MIC1LN and MIC1RN 10: GPIO4 and GPIO5（<800K ） 11: Reserved	RW	00
13:12	OUTSLR	OUTSLR Multiplexing 00: OUTSL and OUTSR 01: MIC1LP and MIC1RP 10: GPIO2 and GPIO3（<800K ） 11: Reserved	RW	00
11:10	OUTSBLR	OUTSBLR Multiplexing 00: OUTSBL and OUTSBR 01: MIC0LN and MIC0RN 10: GPIO0 and GPIO1（<800K ） 11: Reserved	RW	00
9:8	MICINLR	MICINLR multiplexing 00: MICINL and MICINR 01: MIC0LP and MIC0RP 10: DMICCLK and DMICDAT 11:Reserved	RW	00
7:5	TP	TP Multiplexing 111: X1、Y1、X2 and Y2 000: GPIO17、GPIO18、GPIO19 and GPIO20（<1M ） 010: GPIO17、Y1、GPIO19 and GPIO20（<1M ） 100: X1、GPIO18、GPIO19 and GPIO20（<1M ） 110: X1、Y1、GPIO19 and GPIO20（<1M ） others: Reserved	RW	111
4	REMCON	REMCON Multiplexing 0: REMCON 1: GPIO16（<1M ） NOTE：When this signal be used as GPIO16 in a solution, Rem_con_WK_EN bit in SPS_SYS_CTL0 must be cleared before get into standby mode(S2/S3/S4) to avoid waking up	RW	0

		incorrectly.		
3	AUXIN3	AUXIN3 Multiplexing 0: AUXIN3 1: GPIO15（<1M ）	RW	0
2	AUXIN2	AUXIN2 Multiplexing 0: AUXIN2 1: GPIO14（<1M ）	RW	0
1	AUXIN1	AUXIN1 Multiplexing 0: AUXIN1 1: GPIO13（<1M ）	RW	0
0	AUXIN0	AUXIN0 Multiplexing 0: AUXIN0 1: GPIO12（<1M ）	RW	0

Note1: The ( ) follows GPIO function is to indicate the maximum speed of the PAD in GPIO function.More than the speed will affect performance of the ADC DAC and Ethernet mode。It's suggested that the speed of those PAD as slow as possible.

Note2: When bit【11:8】is set to "0110", MIC0 L&R must be disabled, other wise，DMIC PAD and MIC0 LP&RP PAD will conflict each other.

When bit【15:12】is set to "0100", MIC1 L&R must be disabled, other wise，OUTSL&SR PAD and MIC1LP&RP PAD will conflict each other.

When bit【15:12】is set to "0110", MIC1 L&R must be disabled, other wise，GPIO 2&3 PAD and MIC1LP&RP PAD will conflict each other.

Be sure that enable MIC after MFP is set accurately, and before you change the MFP setting you must make MIC disabled

18.4.3 GPIO_OUTEN0

GPIO Output Enable Register 0

Offset=0x10

Bits	Name	Description	R/W	Reset
15:0	GPIO_OUTEN0	GPIO[15:0] Output Enable. 0: Disable 1: Enable	RW	0

18.4.4 GPIO_OUTEN1

GPIO Output Enable Register 1
Offset=0x11

Bits	Name	Description	R/W	Reset
15:0	GPIO_OUTEN1	GPIO[31:16] Output Enable. 0: Disable 1: Enable	RW	0

18.4.5 GPIO_INEN0

GPIO Input Enable Register 0
Offset=0x12

Bits	Name	Description	R/W	Reset
15:0	GPIO_INEN0	GPIO[15:0] Input Enable. 0: Disable 1: Enable	RW	0

18.4.6 GPIO_INEN1

GPIO Input Enable Register 1
Offset=0x13

Bits	Name	Description	R/W	Reset
15:0	GPIO_INEN1	GPIO[31:16] Input Enable. 0: Disable 1: Enable	RW	0

18.4.7 GPIO_DAT0

GPIO Data Register 0
Offset=0x14

Bits	Name	Description	R/W	Reset
15:0	GPIO_DAT0	GPIO[15:0] Input/Output Data.	RW	0

18.4.8 GPIO_DAT1

GPIO Data Register 1
Offset=0x15

Bits	Name	Description	R/W	Reset
15:0	GPIO_DAT1	GPIO[31:16] Input/Output Data.	RW	0

18.4.9 PAD_DRV0

Pad Driving Capacity
Offset=0x20

Bits	Name	Description	R/W	Reset
15:5	-	Reserved	R	0
4	SPI_MISO_DRV	PAD SPI_MISO Drive Capacity 0: Level 2 (MU1=MU2=0) 1: Level 3 (MU1=1,MU2=0)	RW	0
3	I2S_DIN_DRV	AD I2S_DIN Drive Capacity 0: Level 3 (MU1=1, MU2=0) 1 :Level 4 (MU1=MU2=1)	RW	0
2	I2S_DOUT_DRV	PAD I2S_DOUT Drive Capacity 0:Level 3 (MU1=1,MU2=0) 1:Level 4 (MU1=MU2=1)	RW	0
1	DMICCLK_DRV	PAD DMICCLK Drive Capacity 0: Level 2 (analog MU =0) 1: Level 3 (analog MU =1)	RW	0
0	EXTIRQ_DRV	PAD EXTIRQ Drive Capacity 0: Level 2 (MU1=MU2=0) 1: Level 3 (MU1=1,MU2=0)	RW	0

18.4.10 PAD_DRV1

Pad Driving Capacity 1
Offset=0x21

Bits	Name	Description	R/W	Default
15:12	-	Reserved	R	0
11	LED0	PAD LED0 Drive Capacity 0:Level 3 (MU1=1,MU2=0) 1:Level 4 (MU1=MU2=1)	RW	0
10	LED1	PAD LED1 Drive Capacity 0:Level 3 (MU1=1,MU2=0) 1:Level 4 (MU1=MU2=1)	RW	0
9:8	RMII_REF_CLK_DRV	PAD RMII_REF_CLK Drive Capacity 00:Level 2 (MU1=MU2=0) 01:Level 3 (MU1=1,MU2=0) 10:Level 4 (MU1=MU2=1) 11: Reserved	RW	00
7:6	RMII_CRS_DV_DRV	PAD RMII_CRS_DV Drive Capacity 00:Level 2 (MU1=MU2=0) 01:Level 3 (MU1=1,MU2=0) 10:Level 4 (MU1=MU2=1) 11: Reserved	RW	00
5:4	-	Reserved	R	0
3:2	RMII_RXD0_DRV	PAD RMII_RXD0 Drive Capacity 00:Level 2 (MU1=MU2=0) 01:Level 3 (MU1=1,MU2=0) 10:Level 4 (MU1=MU2=1) 11: Reserved	RW	00
1:0	RMII_RXD1_DRV	PAD RMII_RXD1 Drive Capacity 00:Level 2 (MU1=MU2=0) 01:Level 3 (MU1=1,MU2=0) 10:Level 4 (MU1=MU2=1) 11: Reserved	RW	00

18.4.11 PAD_EN

Pad enable control

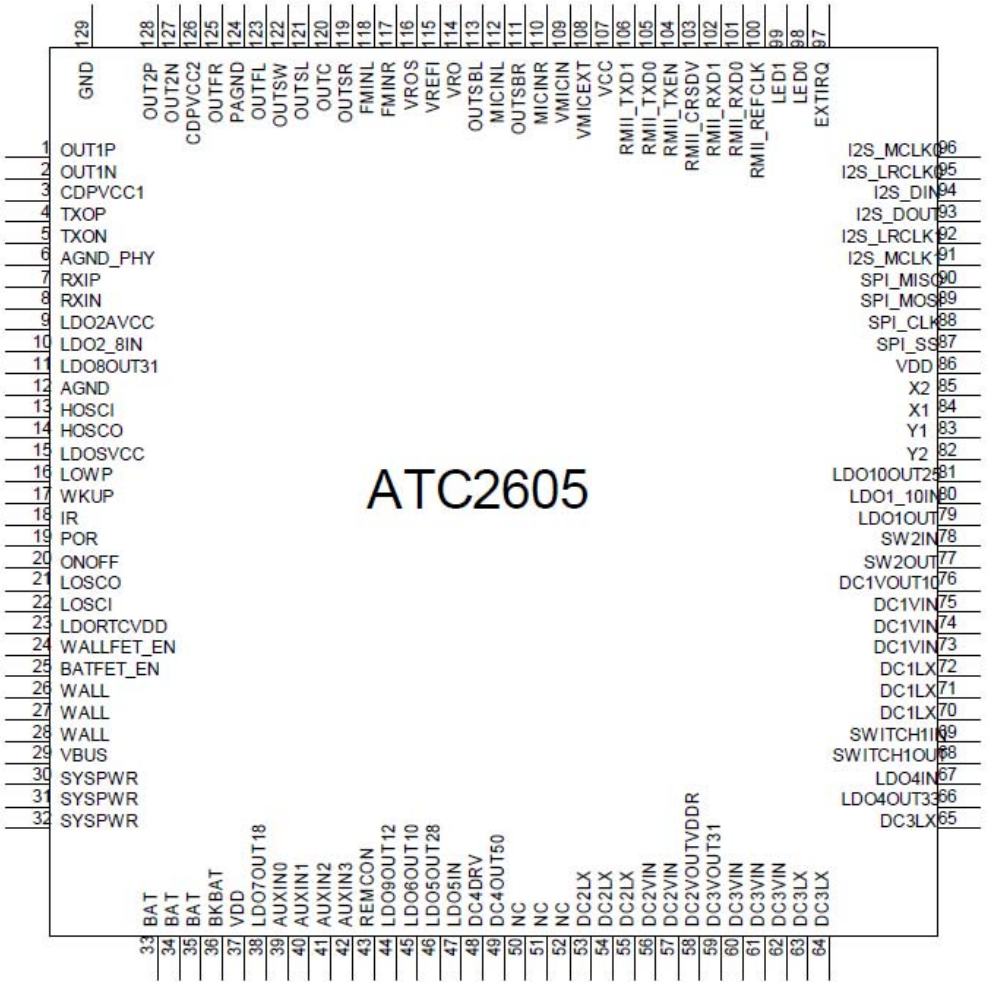
Offset=0x22

Bits	Name	Description	R/W	Default
15:14		Reserved	R	0
13	PAD_EN13	1：P_I2S_MCLK0 pad enable 0：P_I2S_MCLK0 pad disable	RW	0

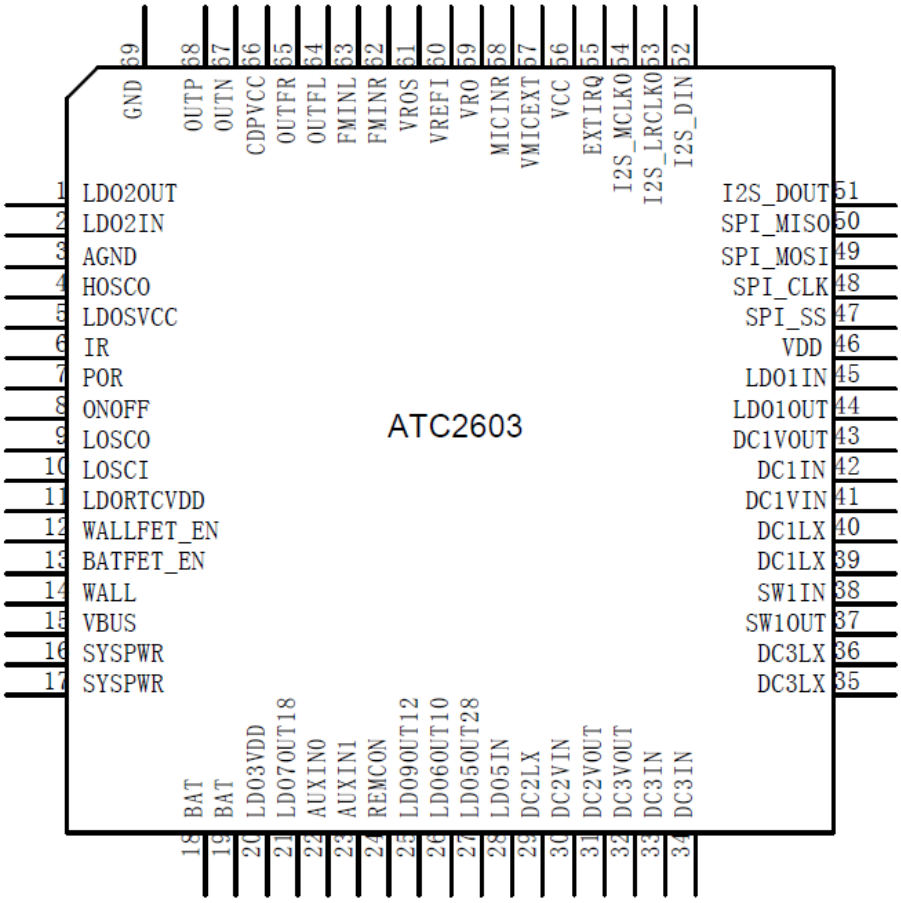
12	PAD_EN12	1：P_I2S_LRCLK0 pad enable 0：P_I2S_LRCLK0 pad disable	RW	0
11	PAD_EN11	1：P_I2S_DIN pad enable 0：P_I2S_DIN pad disable	RW	0
10	PAD_EN10	1：P_I2S_MCLK1 pad enable 0：P_I2S_MCLK1 pad disable	RW	0
9	PAD_EN9	1：P_I2S_LRCLK1 pad enable 0：P_I2S_LRCLK1 pad disable	RW	0
8	PAD_EN8	1：P_I2S_DOUT pad enable 0：P_I2S_DOUT pad disable	RW	0
7	PAD_EN7	1：P_RMII_REF_CLK pad enable 0：P_RMII_REF_CLK pad disable	RW	0
6	PAD_EN6	1：P_RMII_CRS_DV pad enable 0：P_RMII_CRS_DV pad disable	RW	0
5	PAD_EN5	1：P_RMII_RXD0 pad enable 0：P_RMII_RXD0 pad disable	RW	0
4	PAD_EN4	1：P_RMII_RXD1 pad enable 0：P_RMII_RXD1 pad disable	RW	0
3	PAD_EN3	1：P_RMII_TX_EN pad enable 0：P_RMII_TX_EN pad disable	RW	0
2	PAD_EN2	1：P_RMII_TXD0 pad enable 0：P_RMII_TXD0 pad disable	RW	0
1	PAD_EN1	1：P_RMII_TXD1 pad enable 0：P_RMII_TXD1 pad disable	RW	0
0	PAD_EN0	1：P_EXTIRQ pad enable 0：P_EXTIRQ pad disable	RW	0

19. Pin Description

19.1 ATC2605 PinAssignment



19.2 ATC2603 PinAssignment



19.3 ATC2605/ATC2603 Pin Definition

NO.	PIN Name	Function Name	I/O	Description	ATC2605	ATC2603
1	OUT1P	OUT1P	AO	CLASSD1 POSITIVE OUTPUT	1	––
2	OUT1N	OUT1N	AO	CLASSD1 NEGATIVE OUTPUT	2	––
3	CDPVCC1	CDPVCC1	power	CLASSD1 POWER	3	––
4	TXOP	TXOP	AO	Physical transmit signal (+differential)	4	––
5	TXON	TXON	AO	Physical transmit signal (-differential)	5	––
6	AGND_PHY	AGND_PHY	ground	Transmit AGND	6	––
7	RXIP	RXIP	AI	Physical receive signal (+differential)	7	––
8	RXIN	RXIN	AI	Physical receive signal (-differential)	8	––
9	LDO2AVCC	LDO2AVCC	power	Output of voltage regulator LDO2, also for Analog IO use	9	1
10	LDO2_8IN	LDO2_8IN	supply	Input of voltage regulator LDO2	10	2
11	LDO8OUT31	LDO8OUT31	AO	Output of voltage regulator LDO8	11	––
12	AGND	AGND	ground	Analog power ground	12	3
13	HOSCI	HOSCI	AI	Connection for 24/25MHz crystal(output from oscilator to cystal) or 24/25MHz external clock input(when not	13	––

				using crystal)		
14	HOSCO	HOSCO	AO	Connection for 24/25MHz crystal(input to oscilator from cystal)	14	4
15	LDOSVCC	LDOSVCC	power	Output of voltage regulator LDO11, the IO power for standby mode	15	5
16	LOWP	LOWP	DO	DDR S2 ISOLATION SIGNAL	16	––
17	WKUP	WKUP	DI	external wakeup signal input	17	––
18	IR	IR	DI	IR reciver signal	18	6
19	POR	POR	DO	power on reset output to main controller	19	7
20	ONOFF	ONOFF	DI	onoff key input/reset signal	20	8
21	LOSCO	LOSCO	AIO	Crystal Oscillator Input of 32.768KHz	21	9
22	LOSCI	LOSCI	AI	Crystal Oscillator output of 32.768KHz	22	10
23	LDORTCVDD	LDORTCVDD	power	Output of voltage regulator LDO12	23	11
24	WALLFET_EN	WALLFET_EN	AO	Gate signal of external MOSFET connected to WALL	24	12
25	BATFET_EN	BATFET_EN	AO	Gate signal of external MOSFET connected to BAT	25	13
26	WALL	WALL	supply	Connected to wall adapter power	26	

				supply		
27	WALL	WALL	supply	Connected to wall adapter power supply	27	14
28	WALL	WALL	supply	Connected to wall adapter power supply	28	––
29	VBUS	VBUS	supply	Connected to USB power supply	29	15
30	SYSPWR	SYSPWR	power	SYSTEM POWER	30	16
31	SYSPWR	SYSPWR	power	SYSTEM POWER	31	17
32	SYSPWR	SYSPWR	power	SYSTEM POWER	32	
33	BAT	BAT	supply	Connected to battery power supply	33	18
34	BAT	BAT	supply	Connected to battery power supply	34	19
35	BAT	BAT	supply	Connected to battery power supply	35	––
36	BKBAT	BKBAT	supply	bakeup battrey power supply	36	––
37	VDD	VDD	power	Core logic power	37	20
38	LDO7OUT18	LDO7OUT18	AO	Output of voltage regulator LDO7	38	21
39	AUXIN0	AUXIN0	AIO	gerenal ADC input0	39	22
40	AUXIN1	AUXIN1	AIO	gerenal ADC input1	40	23
41	AUXIN2	AUXIN2	AIO	gerenal ADC input2	41	––
42	AUXIN3	AUXIN3	AIO	gerenal ADC input3	42	––
43	REMCON	REMCON	AIO	gerenal ADC input4, for remote control	43	24
44	LDO9OUT12	LDO9OUT12	AO	Output of voltage regulator LDO9	44	25
45	LDO6OUT10	LDO6OUT10	AO	Output of voltage regulator LDO6	45	26

46	LDO5OUT28	LDO5OUT28	AO	Output of voltage regulator LDO5	46	27
47	LDO5IN	LDO5IN	supply	Input of voltage regulator LDO5	47	28
48	DC4DRV	DC4DRV	AO	DC-DC4 drive pin	48	––
49	DC4OUT50	DC4OUT50	AO	DC-DC4	49	––
50	DC5DRV	DC5DRV	AO	DC-DC5 drive pin	50	––
51	DC5FBLED	DC5FBLED	AI	DC-DC5 feedback pin	51	––
52	ILED	ILED	AI		52	––
53	DC2LX	DC2LX	AO	DC-DC2 inductor connection	53	––
54	DC2LX	DC2LX	AO	DC-DC2 inductor connection	54	––
55	DC2LX	DC2LX	AO	DC-DC2 inductor connection	55	29
56	DC2VIN	DC2VIN	supply	DC-DC2 power input	56	30
57	DC2VIN	DC2VIN	supply	DC-DC2 power input	57	––
58	DC2VOUTVDDR	DC2VOUTVDDR	AO	Output of DC-DC2	58	31
59	DC3VOUT31	DC3VOUT31	power	Output of DC-DC3	59	32
60	DC3VIN	DC3VIN	supply	DC-DC3 power input	60	33
61	DC3VIN	DC3VIN	supply	DC-DC3 power input	61	34
62	DC3VIN	DC3VIN	supply	DC-DC3 power input	62	––
63	DC3LX	DC3LX	AO	DC-DC3 inductor connection	63	35
64	DC3LX	DC3LX	AO	DC-DC3 inductor connection	64	36
65	DC3LX	DC3LX	AO	DC-DC4 inductor connection	65	––
66	LDO4OUT33	LDO4OUT33	AO	Output of voltage regulator LDO4	66	––

67	LDO4IN	LDO4IN	supply	Input of voltage regulator LDO4	67	--
68	SWITCH1OUT	SWITCH1OUT	power	Output of voltage regulator Switch1	68	37
69	SWITCH1IN	SWITCH1IN	supply	Input of voltage regulator Switch1	69	38
70	DC1LX	DC1LX	AO	DC-DC1 inductor connection	70	39
71	DC1LX	DC1LX	AO	DC-DC1 inductor connection	71	--
72	DC1LX	DC1LX	AO	DC-DC1 inductor connection	72	40
73	DC1VIN	DC1VIN	supply	DC-DC1 power input	73	41
74	DC1VIN	DC1VIN	supply	DC-DC1 power input	74	42
75	DC1VIN	DC1VIN	supply	DC-DC1 power input	75	--
76	DC1VOUT10	DC1VOUT10	power	Output of DC-DC1	76	43
77	SW2OUT	SW2OUT	power	Output of voltage regulator Switch2	77	--
78	SW2IN	SW2IN	supply	Input of voltage regulator Switch2	78	--
79	LDO1OUT	LDO1OUT	AO	Output of voltage regulator LDO1	79	44
80	LDO1_10IN	LDO1_10IN	supply	Input of voltage regulator LDO1&LDO10	80	45
81	LDO10OUT25	LDO10OUT25	AO	Output of voltage regulator LDO10	81	--
82	Y2	Y2	AIO	Touch Panel Y2	82	--
		GPIO20		General Purpose Input/Output 20		
83	Y1	Y1	AIO	Touch Panel Y1	83	--
		GPIO18		General Purpose Input/Output 18		
84	X1	X1	AIO	Touch Panel X1	84	--
		GPIO17		General Purpose Input/Output 17		

85	X2	X2	AIO	Touch Panel X2	85	––
		GPIO19		General Purpose Input/Output 19		
86	VDD	VDD	power	Core logic power	86	46
87	SPI_SS	SPI_SS	DI	SPI Slave Select	87	47
88	SPI_CLK	SPI_CLK	DI	SPI Slave clock	88	48
89	SPI_MOSI	SPI_MOSI	DI	SPI Slave input	89	49
90	SPI_MISO	SPI_MISO	DO	SPI Slave output	90	50
91	I2S_MCLK1	I2S_MCLK1	DIO	I2S MASTER CLOCK1	91	––
		GPIO9		General Purpose Input/Output 9		
92	I2S_LRCLK1	I2S_LRCLK1	DIO	I2S LR CLOCK1	92	––
		GPIO10		General Purpose Input/Output 10		
93	I2S_DOUT	I2S_DOUT	DIO	I2S DATA OUTPUT	93	51
		GPIO11		General Purpose Input/Output 11		
94	I2S_DIN	I2S_DIN	DIO	I2S DATA INPUT	94	52
		I2S_DOUT		I2S DATA OUTPUT		
		GPIO8		General Purpose Input/Output 8		
95	I2S_LRCLK0	I2S_LRCLK0	DIO	I2S LR CLOCK0	95	53
		GPIO7		General Purpose Input/Output 7		
96	I2S_MCLK0	I2S_MCLK0	DIO	I2S MASTER CLOKCK0	96	54
		GPO6		General Purpose Input/Output 6		
97	EXTIRQ	EXTIRQ	DO	IRQ outpur signal	97	55
98	LED0	LED0	DIO	Link LED/Traffic LED	98	––
99	LED1	LED1	DIO	Link speed LED	99	––

100	RMII_REFCLK	RMII_REFCLK	DIO	RMII Synchronous 50MHz clock reference for receive, transmit and control interface.	100	--
		SMII_CLK		SMII Synchronous 125MHz clock reference for receive, transmit and control interface.		
		GPIO21		General Purpose Input/Output 21		
101	RMII_RXD0	RMII_RXD0	DIO	RMII Receive Data0;	101	--
		GPIO23		General Purpose Input/Output 23		
102	RMII_RXD1	RMII_RXD1	DIO	RMII Receive Data1	102	--
		GPIO24		General Purpose Input/Output 24		
103	RMII_CRSDV	RMII_CRSDV	DIO	RMII Carrier Sense/Receive Data Valid	103	--
		SMII_RX		SMII Receive Data		
		GPIO22		General Purpose Input/Output 22		
104	RMII_TXEN	RMII_TXEN	DIO	RMII Transmit enable	104	--
		GPIO25		General Purpose Input/Output 25		
105	RMII_TXD0	RMII_TXD0	DIO	RMII Transmit Data0;	105	--
		SMII_TX		SMII Transmit Data		
		GPIO26		General Purpose Input/Output 26		
106	RMII_TXD1	RMII_TXD1	DIO	RMII Transmit Data1;	106	--
		SMII_SYNC		SMII Synchronization		

		GPIO27		General Purpose Input/Output 27		
107	VCC	VCC	power	Digital IO power	107	56
108	VMICEXT	VMICEXT	AO	EXTERNAL MIC BIAS	108	57
109	VMICIN	VMICIN	AO	INTERNAL MIC BIAS	109	––
110	MICINR	MICINR	AI	MICR CHANNEL INPUT	110	58
		MIC0RP		MIC0R Positive CHANNEL INPUT when use as differential		
		DMICDAT		Data signal of digital mic		
111	OUTSBR	OUTSBR	AIO	BACK SURROUND RIGHT CHANNEL OUTPUT	111	––
		MIC0RN		MIC0R Negetive CHANNEL INPUT when use as differential		
		GPIO1		General Purpose Input/Output 1		
112	MICINL	MICINL	AI	MICL CHANNEL INPUT	112	––
		MIC0LP		MIC0L Positive CHANNEL INPUT when use as differential		
		DMICCLK		Clock signal of digital mic		
113	OUTSBL	OUTSBL	AIO	BACK SURROUND LEFT CHANNEL OUTPUT	113	––
		MIC0LN		MIC0L Negetive CHANNEL INPUT when use as		

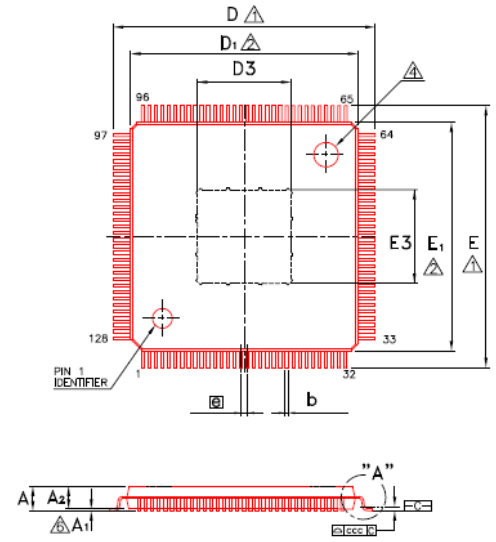
				differential		
		GPIO0		General Purpose Input/Output 0		
114	VRO	VRO	AO	VR OUTPUT	114	59
115	VREFI	VREFI	AIO	Reference Voltage,with capacitance	115	60
116	VROS	VROS	AO	VRO SENSE	116	61
117	FMINR	FMINR	AI	FMR CHANNEL INPUT	117	62
118	FMINL	FMINL	AI	FML CHANNEL INPUT	118	63
119	OUTSR	OUTSR	AIO	SURROUND RIGHT CHANNEL OUTPUT	119	––
		MIC1RP		MIC1R Positive CHANNEL INPUT when use as differential		
		GPIO3		General Purpose Input/Output 3		
120	OUTC	OUTC	AIO	CENTER CHANNEL OUTPUT	120	––
		MIC1RN		MIC1R Negetive CHANNEL INPUT when use as differential		
		GPIO5		General Purpose Input/Output 5		
121	OUTSL	OUTSL	AIO	SURROUND LEFT CHANNEL OUTPUT	121	––
		MIC1LP		MIC1L Positive CHANNEL INPUT when use as differential		

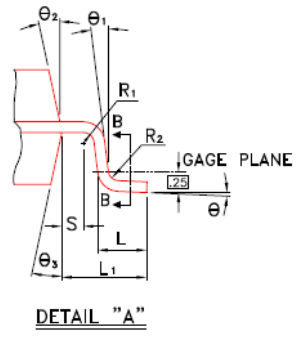
		GPIO2		General Purpose Input/Output 2		
122	OUTSW	OUTSW	AIO	SUBWOOFER CHANNEL OUTPUT	122	––
		MIC1LN		MIC1L Negetive CHANNEL INPUT when use as differential		
		GPIO4		General Purpose Input/Output 4		
123	OUTFL	OUTFL	AO	FRONT LEFT CHANNEL OUTPUT	123	64
124	PAGND	PAGND	ground	Ground of PA power	124	––
125	OUTFR	OUTFR	AO	FRONT RIGHT CHANNEL OUTPUT	125	65
126	CDPVCC2	CDPVCC2	power	CLASSD2 POWER	126	66
127	OUT2N	OUT2N	AO	CLASSD2 NEGATIVE OUTPUT	127	67
128	OUT2P	OUT2P	AO	CLASSD2 POSITIVE OUTPUT	128	68

20 Package and Ordering Information

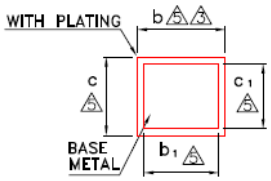
20.1 Package Drawing

ATC2605 Package Drawing





DETAIL "A"

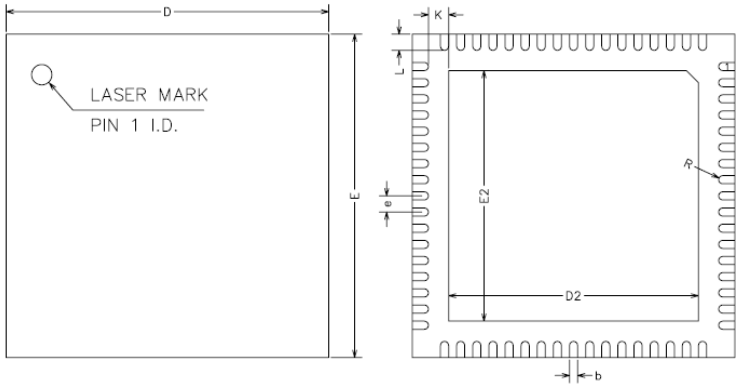


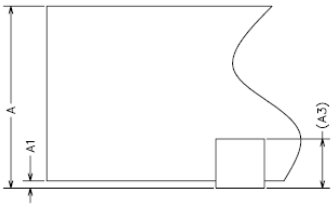
SECTION B-B

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	—	0.002	—	—
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	12°TYP			12°TYP		
θ3	12°TYP			12°TYP		
ccc	0.08			0.003		

Exposed Pad Size			
L/F		Dimension in mm	Dimension in inch
①	D3/E3	3.61 REF	0.142 REF
②	D3/E3	5.72 REF	0.225 REF
③	D3/E3	8.00 REF	0.315 REF
④	D3/E3	7.75 / 6.60 REF	0.305 / 0.260 REF

ATC2603 Package Drawing





COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20REF	
b	0.15	0.20	0.25
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	6.10	6.20	6.30
E2	6.10	6.20	6.30
e	0.30	0.40	0.50
K	0.20	–	–
L	0.35	0.40	0.45
R	0.09	–	–

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