

High-voltage, high-side current sense amplifier

Features

- Independent supply and input common-mode voltages
- Wide common-mode operating range:
2.9 to 70 V in single-supply configuration,
-2.1 to 65 V in dual-supply configuration
- Wide common-mode surviving range:
-16 to 75 V (reversed battery and load-dump conditions)
- Supply voltage range:
2.7 to 5.5 V in single-supply configuration
- Low current consumption: I_{CC} max = 360 μ A
- Pin selectable gain: 20 V/V, 25 V/V, 50 V/V or 100 V/V
- Buffered output

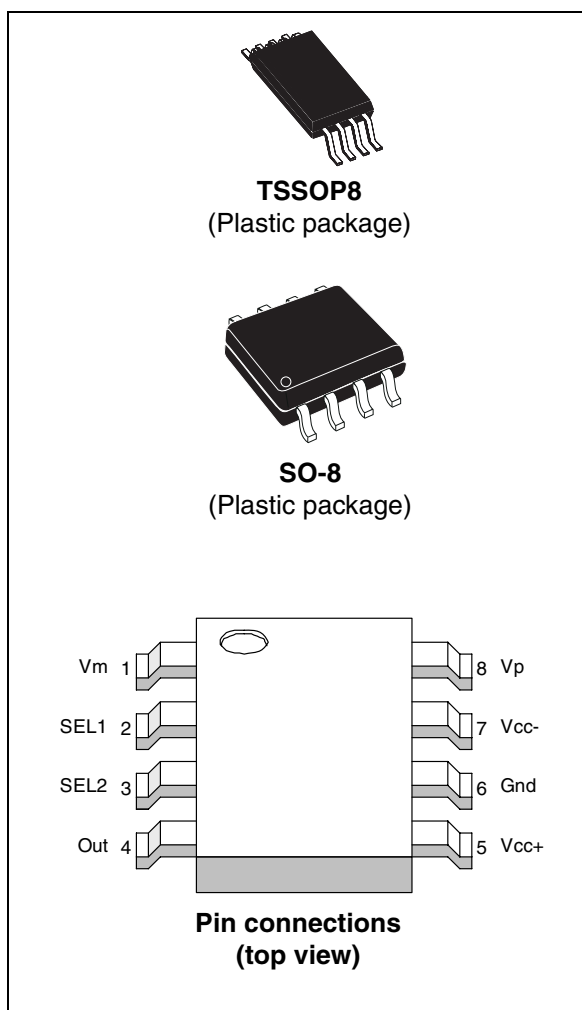
Applications

- Automotive current monitoring
- DC motor control
- Photovoltaic systems
- Battery chargers
- Precision current sources
- Current monitoring of notebook computers
- Uninterruptible power supplies
- High-end power supplies

Description

The TSC103 measures a small differential voltage on a high-side shunt resistor and translates it into a ground-referenced output voltage. The gain is adjustable to four different values from 20 V/V up to 100 V/V by two selection pins.

Wide input common-mode voltage range, low quiescent current, and tiny TSSOP8 packaging enable use in a wide variety of applications.



The input common-mode and power-supply voltages are independent. The common-mode voltage can range from 2.9 to 70 V in the single-supply configuration or be offset by an adjustable voltage supplied on the Vcc- pin in the dual-supply configuration.

With a current consumption lower than 360 μ A and a virtually null input leakage current in standby mode, the power consumption in the applications is minimized.

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1 Application schematic and pin description

The TSC103 high-side current sense amplifier can be used in either single- or dual-supply mode. In the single-supply configuration, the TSC103 features a wide 2.9 V to 70 V input common-mode range totally independent of the supply voltage. In the dual-supply range, the common-mode range is shifted by the value of the negative voltage applied on the Vcc- pin. For instance, with Vcc+ = 5 V and Vcc- = -5 V, then the input common-mode range is -2.1 V to 65 V.

Figure 1. Single-supply configuration schematic

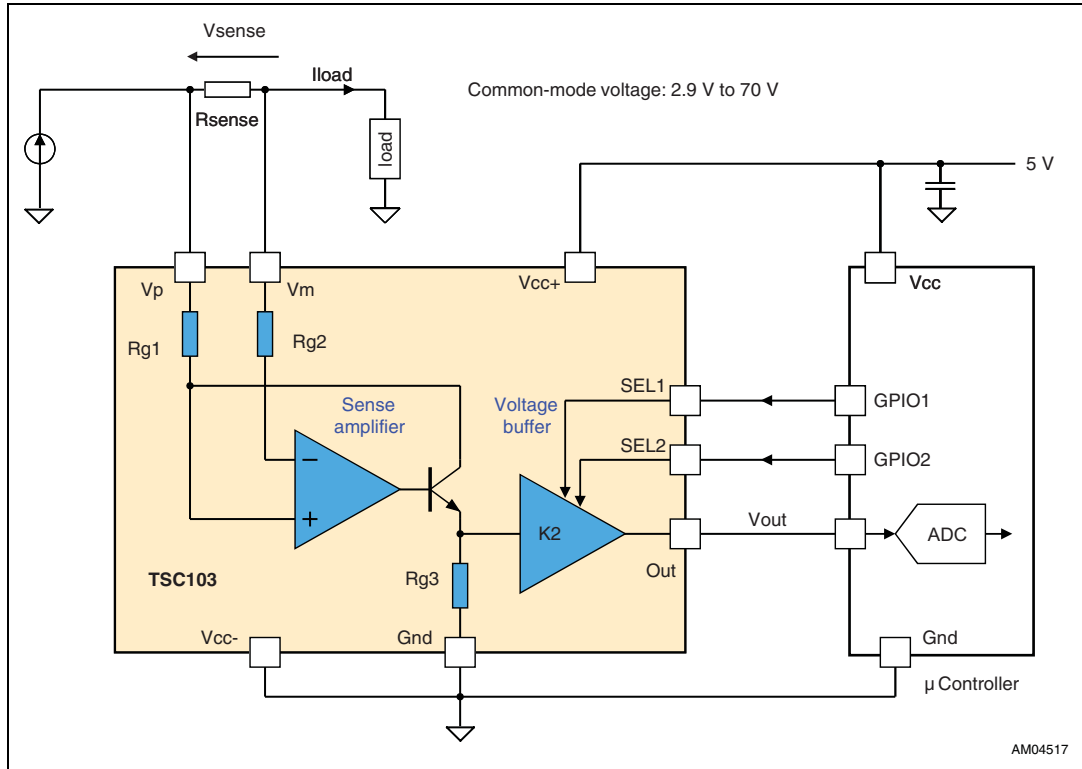


Figure 2. Dual-supply configuration schematic

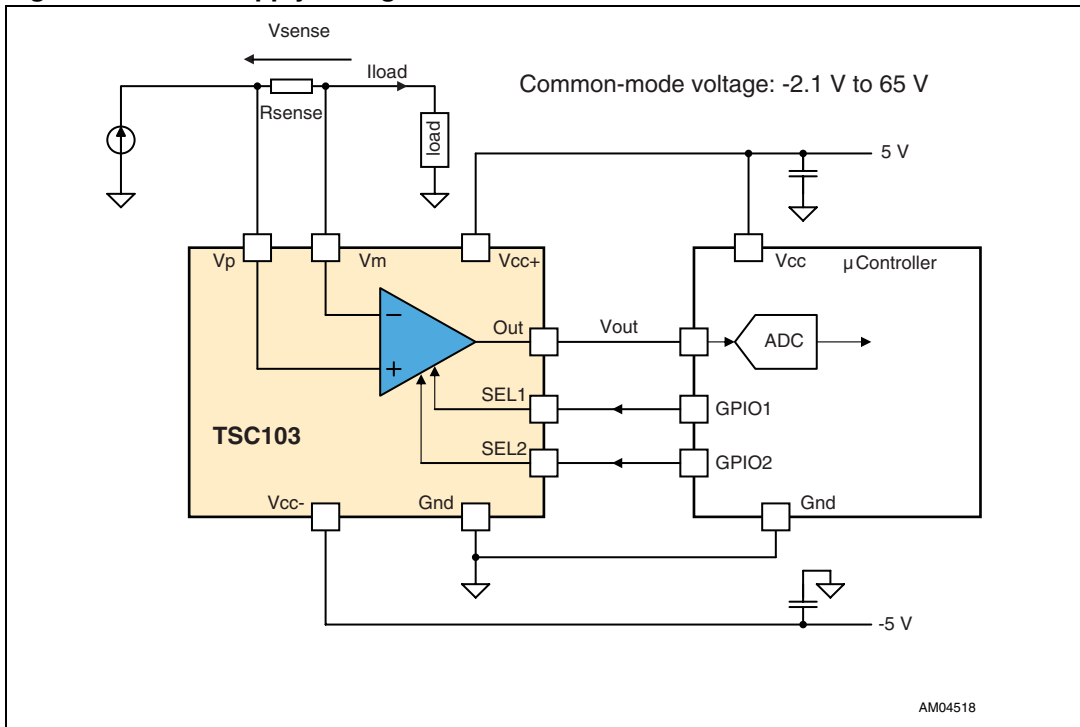


Figure 3. Common-mode versus supply voltage in dual-supply configuration

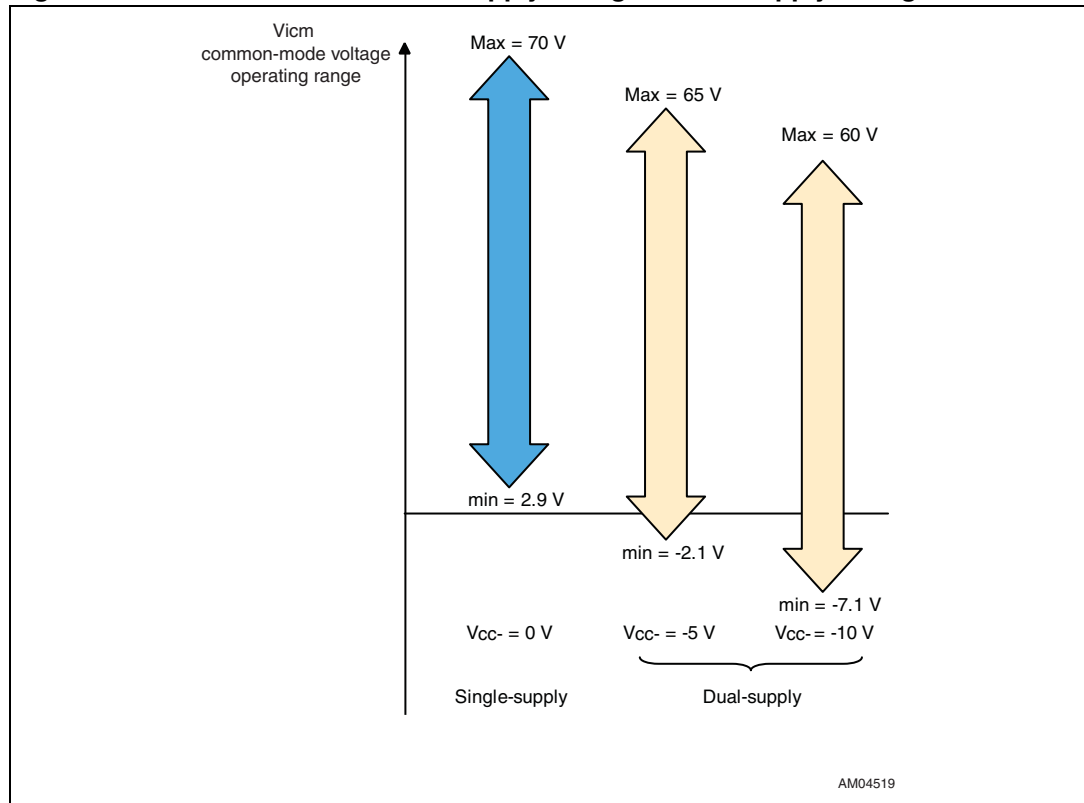


Table 1 describes the function of each pin. Their position is shown in the illustration on the cover page and in Figure 1 on page 3.

Table 1. Pin description

| Symbol | Type | Function |
|--------|---------------|--|
| Out | Analog output | The Out voltage is proportional to the magnitude of the sense voltage $V_p - V_m$. |
| Gnd | Power supply | Ground line. |
| Vcc+ | Power supply | Positive power supply line. |
| Vcc- | Power supply | Negative power supply line. |
| Vp | Analog input | Connection for the external sense resistor. The measured current enters the shunt on the V_p side. |
| Vm | Analog input | Connection for the external sense resistor. The measured current exits the shunt on the V_m side. |
| SEL1 | Digital input | Gain-select pin. |
| SEL2 | Digital input | Gain-select pin. |

2 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|---------------------|--|-------------------------|------|
| V_{id} | Input pins differential voltage ($V_p - V_m$) | ± 20 | V |
| V_{in_sense} | Sensing pins input voltages (V_p, V_m) ⁽¹⁾ | -16 to 75 | V |
| V_{in_sel} | Gain selection pins input voltages (SEL1, SEL2) ⁽²⁾ | -0.3 to $V_{CC+} + 0.3$ | V |
| V_{CC+} | Positive supply voltage ⁽²⁾ | -0.3 to 7 | V |
| $V_{CC+} - V_{CC-}$ | DC supply voltage | 0 to 15 | V |
| V_{out} | DC output pin voltage ⁽²⁾ | -0.3 to $V_{CC+} + 0.3$ | V |
| T_{stg} | Storage temperature | -55 to 150 | °C |
| T_j | Maximum junction temperature | 150 | °C |
| R_{thja} | TSSOP8 thermal resistance junction to ambient | 120 | °C/W |
| | SO-8 thermal resistance junction to ambient | 125 | °C/W |
| ESD | HBM: human body model ⁽³⁾ | 2.5 | kV |
| | MM: machine model ⁽⁴⁾ | 150 | V |
| | CDM: charged device model ⁽⁵⁾ | 1.5 | kV |

1. These voltage values are measured with respect to the V_{CC-} pin.
2. These voltage values are measured with respect to the Gnd pin.
3. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
4. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
5. Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to ground.

Table 3. Operating conditions

| Symbol | Parameter | Value | Unit |
|------------|---|------------|------|
| V_{CC+} | Supply voltage in single-supply configuration from T_{min} to T_{max} (V_{CC-} connected to Gnd = 0 V) | 2.7 to 5.5 | V |
| V_{CC-} | Negative supply voltage in dual-supply configuration from T_{min} to T_{max} | | |
| | $V_{CC+} = 5.5$ V max | -8 to 0 | V |
| | $V_{CC+} = 3$ V max | -11 to 0 | V |
| V_{icm} | Common-mode voltage range referred to pin V_{CC-} (T_{min} to T_{max}) | 2.9 to 70 | V |
| T_{oper} | Operational temperature range (T_{min} to T_{max}) | -40 to 125 | °C |

3 Electrical characteristics

The electrical characteristics given in the following tables are measured under the following test conditions unless otherwise specified.

- $T_{amb} = 25^{\circ} \text{C}$, $V_{CC+} = 5 \text{ V}$, V_{CC-} connected to Gnd (single-supply configuration).
- $V_{sense} = V_p - V_m = 50 \text{ mV}$, $V_m = 12 \text{ V}$, no load on Out, all gain configurations.

Table 4. Supply

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------|----------------------|---|------|------|------|---------------|
| I_{CC} | Total supply current | $V_{sense} = 0 \text{ V}$, $T_{min} < T_{amb} < T_{max}$ | | 200 | 360 | μA |
| I_{CC1} | Total supply current | $V_{sense} = 50 \text{ mV}$ $A_v = 50 \text{ V/V}$ $T_{min} < T_{amb} < T_{max}$ | | 300 | 480 | μA |

Table 5. Input

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|--|--|------|------|-------------------------|--------------------------------|
| DC CMR | DC common-mode rejection Variation of V_{out} versus V_{icm} referred to input ⁽¹⁾ | $2.9 \text{ V} < V_m < 70 \text{ V}$ $T_{min} < T_{amb} < T_{max}$ | 90 | 105 | | dB |
| AC CMR | AC common-mode rejection Variation of V_{out} versus V_{icm} referred to input (peak-to-peak voltage variation) | $A_v = 50 \text{ V/V}$ or 100 V/V $2.9 \text{ V} < V_m < 30 \text{ V}$ 1 kHz sine wave | | 95 | | dB |
| SVR | Supply voltage rejection Variation of V_{out} versus V_{CC} ⁽²⁾ SEL1 = Gnd, SEL2 = Gnd | $2.7 \text{ V} < V_{CC} < 5.5 \text{ V}$ $V_{sense} = 30 \text{ mV}$ $T_{min} < T_{amb} < T_{max}$ | 85 | 95 | | dB |
| V_{os} | Input offset voltage ⁽³⁾ | $T_{amb} = 25^{\circ} \text{C}$ $T_{min} < T_{amb} < T_{max}$ | | | ± 500 ± 1100 | μV |
| dV_{os}/dT | Input offset drift vs. T | $A_v = 50 \text{ V/V}$ $T_{min} < T_{amb} < T_{max}$ | -20 | | +5 | $\mu\text{V}/^{\circ}\text{C}$ |
| I_{lk} | Input leakage current | $V_{CC} = 0 \text{ V}$ $T_{min} < T_{amb} < T_{max}$ | | | 1 | μA |
| I_{ib} | Input bias current | $V_{sense} = 0 \text{ V}$ $T_{min} < T_{amb} < T_{max}$ | | 10 | 15 | μA |
| V_{IL} | Logic low voltage threshold (SEL1 and SEL2) | $V_{CCmin} < V_{CC} < V_{CCmax}$ $T_{min} < T_{amb} < T_{max}$ | -0.3 | | 0.5 | V |
| V_{IH} | Logic high voltage threshold (SEL1 and SEL2) | $V_{CCmin} < V_{CC} < V_{CCmax}$ $T_{min} < T_{amb} < T_{max}$ | 1.2 | | V_{CC} | V |
| I_{sel} | Gain-select pins (SEL1 and SEL2) input bias current | SEL pin connected to GND or V_{CC} $T_{min} < T_{amb} < T_{max}$ | | 400 | | nA |

1. See [Chapter 5: Parameter definitions on page 13](#) for the definition of CMR.

2. See [Chapter 5](#) for the definition of SVR.

3. See [Chapter 5](#) for the definition of V_{os} .

Table 6. Output

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------------------------|---|--|------|-----------------------|------------|--------|
| A_v | Gain | SEL1 = Gnd, SEL2 = Gnd SEL1 = Gnd, SEL2 = Vcc+ SEL1 = Vcc+, SEL2 = Gnd SEL1 = Vcc+, SEL2 = Vcc+ | | 20 25 50 100 | | V/V |
| $\Delta V_{out}/\Delta T$ | Output voltage drift vs. T ⁽¹⁾ | $A_v = 50 \text{ V/V}$ $T_{min} < T_{amb} < T_{max}$ | | | ±240 | ppm/°C |
| $\Delta V_{out}/\Delta I_{out}$ | Output stage load regulation | -10 mA < I_{out} < 10 mA I_{out} sink or source current $A_v = 50 \text{ V/V}$ | | 0.3 | ±1.5 | mV/mA |
| ΔV_{out} | Total output voltage accuracy ⁽²⁾ | $V_{sense} = 50 \text{ mV}^{(3)}$ $T_{amb} = 25^\circ \text{C}$ $T_{min} < T_{amb} < T_{max}$ | | | ±2.5 ±4 | % |
| ΔV_{out} | Total output voltage accuracy | $V_{sense} = 90 \text{ mV}^{(3)}$ $T_{amb} = 25^\circ \text{C}$ $T_{min} < T_{amb} < T_{max}$ | | | ±3.5 ±5 | % |
| ΔV_{out} | Total output voltage accuracy | $V_{sense} = 20 \text{ mV}$ $T_{amb} = 25^\circ \text{C}$ $T_{min} < T_{amb} < T_{max}$ | | | ±3.5 ±5 | % |
| ΔV_{out} | Total output voltage accuracy | $V_{sense} = 10 \text{ mV}$ $T_{amb} = 25^\circ \text{C}$ $T_{min} < T_{amb} < T_{max}$ | | | ±5.5 ±8 | % |
| ΔV_{out} | Total output voltage accuracy | $V_{sense} = 5 \text{ mV}$ $T_{amb} = 25^\circ \text{C}$ $T_{min} < T_{amb} < T_{max}$ | | | ±10 ±22 | % |
| I_{sc} | Short-circuit current | OUT connected to V _{CC} or GND | 15 | 26 | | mA |
| V_{OH} | Output stage high-state saturation voltage $V_{OH} = V_{CC} - V_{out}$ | $V_{sense} = 1 \text{ V}$ $I_{out} = 1 \text{ mA}$ | | 85 | 135 | mV |
| V_{OL} | Output stage low-state saturation voltage | $V_{sense} = -1 \text{ V}$ $I_{out} = 1 \text{ mA}$ | | 80 | 125 | mV |

1. See [Chapter 5: Parameter definitions on page 13](#) for the definition of output voltage drift versus temperature.
2. Output voltage accuracy is the difference with the expected theoretical output voltage $V_{out-th} = A_v \cdot V_{sense}$. See [Chapter 5](#) for a more detailed definition.
3. Except for $A_v = 100 \text{ V/V}$.

Table 7. Frequency response

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------------|--|---|------|------|------|------|
| ts | Response to input differential voltage change. Output settling to 1% of final value | V _{sense} square pulse applied to generate a variation of V _{out} from 500 mV to 3 V C _{load} = 47 pF | | | | |
| | | Av = 20 V/V, | | 3 | | μs |
| | | Av = 25 V/V | | 4 | | μs |
| | | Av = 50 V/V | | 6 | | μs |
| | | Av = 100 V/V | | 10 | | μs |
| t _{SEL} | Response to a gain change. Output settling to 1% of final value | Any change of state of SEL1 or SEL2 pin | | 1 | | μs |
| t _{rec} | Response to common-mode voltage change. Output settling to 1% of final value | V _{CC+} = 5 V, V _{CC-} = -5 V V _m step change from -2 V to 30 V or 30 V to -2 V | | 20 | | μs |
| SR | Slew rate | V _{sense} = 10 mV to 100 mV | 0.4 | 0.6 | | V/μs |
| BW | 3 dB bandwidth | C _{load} = 47 pF V _m = 12 V V _{sense} = 50 mV Av = 50 V/V | | 700 | | kHz |

Table 8. Noise

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------|--------------------------------|-----------------|------|------|------|--------|
| e _N | Equivalent input noise voltage | f = 1 kHz | | 40 | | nV/√Hz |

4 Electrical characteristics curves: current sense amplifier

Unless otherwise specified, the test conditions for the following curves are:

- $T_{amb} = 25^{\circ}\text{C}$, $V_{CC} = 5\text{ V}$, $V_{sense} = V_p - V_m = 50\text{ mV}$, $V_m = 12\text{ V}$.
- No load on Out pin.

Figure 4. Output voltage vs. V_{sense}

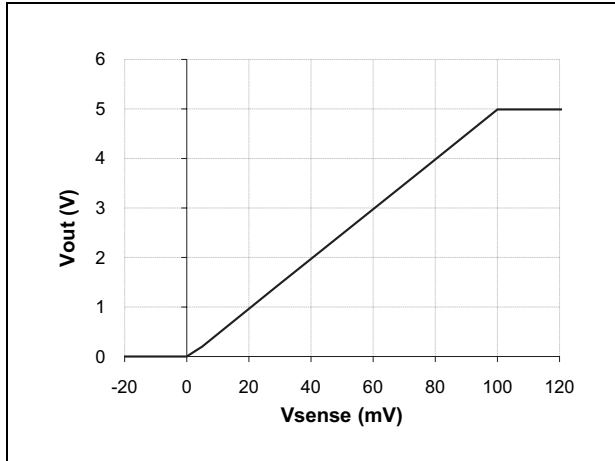


Figure 5. Output voltage accuracy vs. V_{sense}

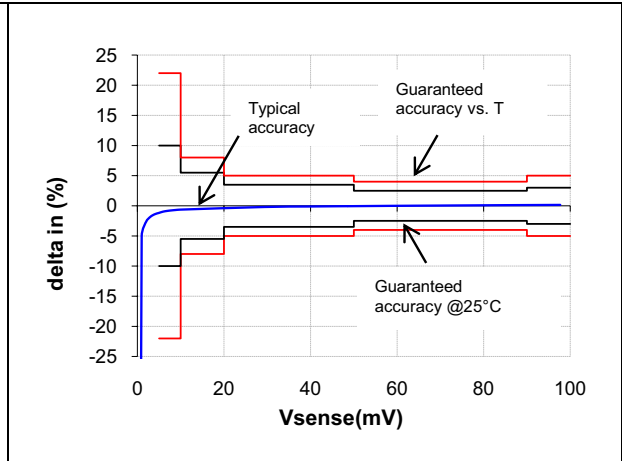


Figure 6. Supply current vs. supply voltage

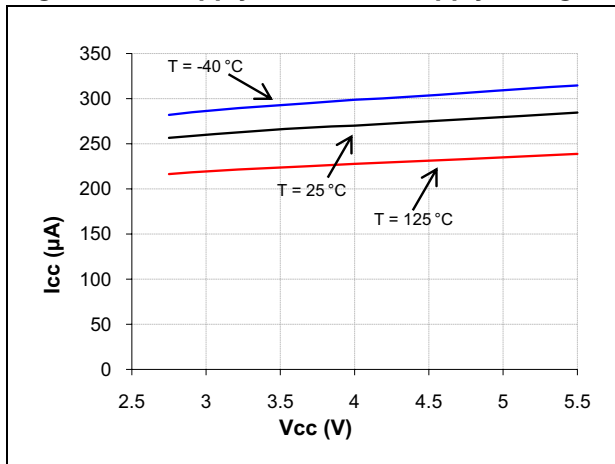


Figure 7. Supply current vs. V_{sense}

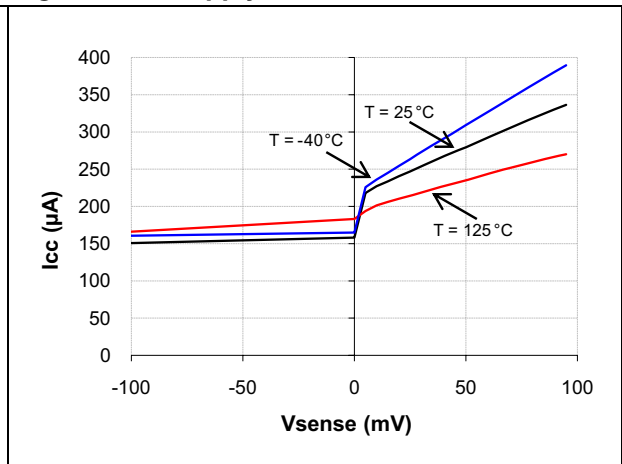


Figure 8. V_p pin input current vs. V_{sense}

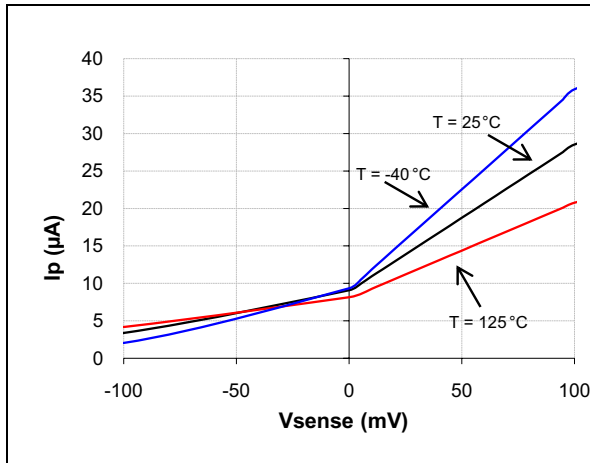


Figure 9. V_n pin input current vs. V_{sense}

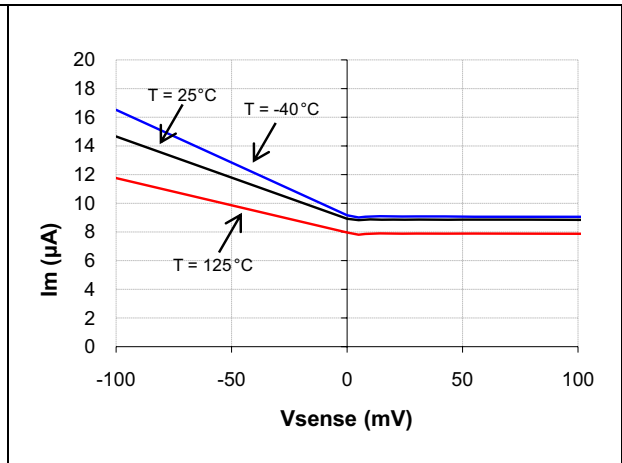


Figure 10. Output stage low-state saturation voltage vs. output current ($V_{sense} = -1 V$)

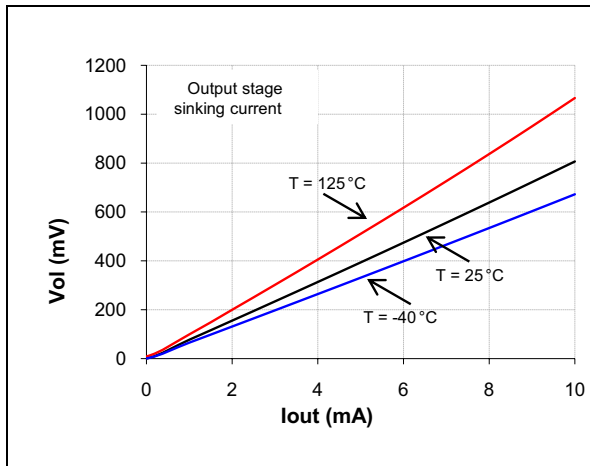


Figure 11. Output stage high-state saturation voltage vs. output current ($V_{sense} = +1 V$)

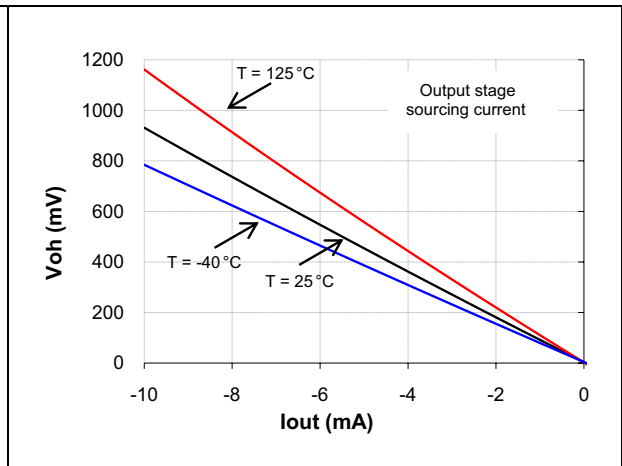


Figure 12. Output stage load regulation

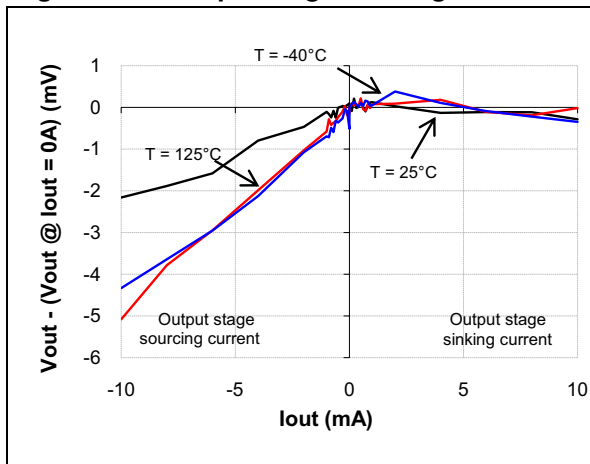


Figure 13. Step response

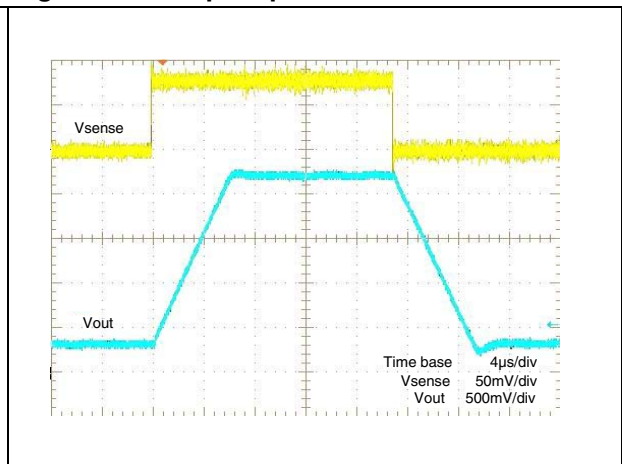


Figure 14. Bode diagram

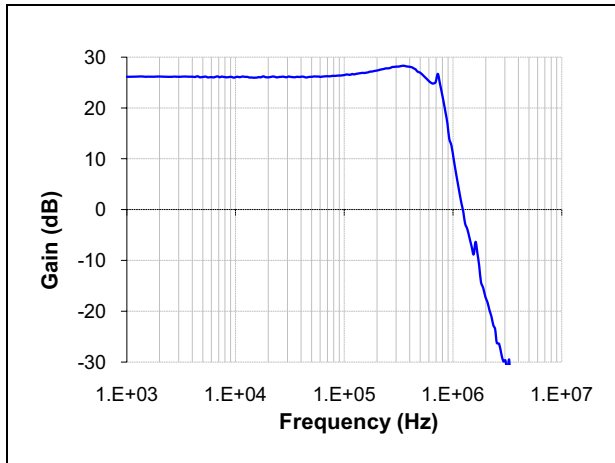


Figure 15. Power supply rejection ratio

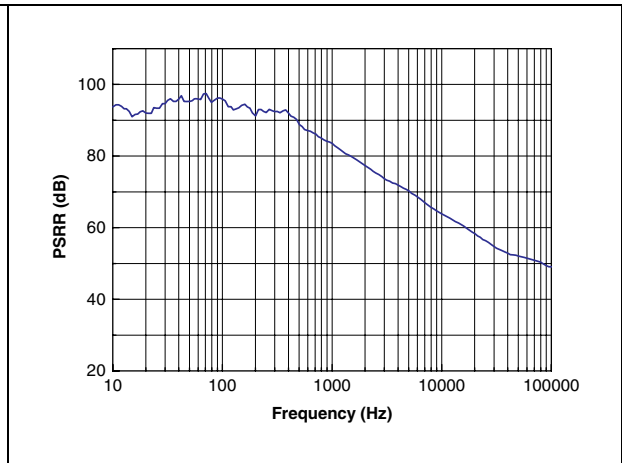
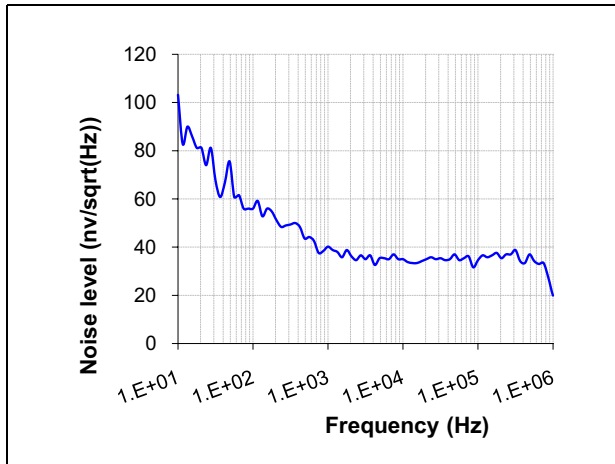


Figure 16. Noise level



5 Parameter definitions

5.1 Common mode rejection ratio (CMR)

The common-mode rejection ratio (CMR) measures the ability of the current-sensing amplifier to reject any DC voltage applied on both inputs V_p and V_m . The CMR is referred back to the input so that its effect can be compared with the applied differential signal. The CMR is defined by the formula:

$$\text{CMR} = -20 \cdot \log \frac{\Delta V_{\text{out}}}{\Delta V_{\text{icm}} \cdot A_v}$$

5.2 Supply voltage rejection ratio (SVR)

The supply-voltage rejection ratio (SVR) measures the ability of the current-sensing amplifier to reject any variation of the supply voltage V_{CC} . The SVR is referred back to the input so that its effect can be compared with the applied differential signal. The SVR is defined by the formula:

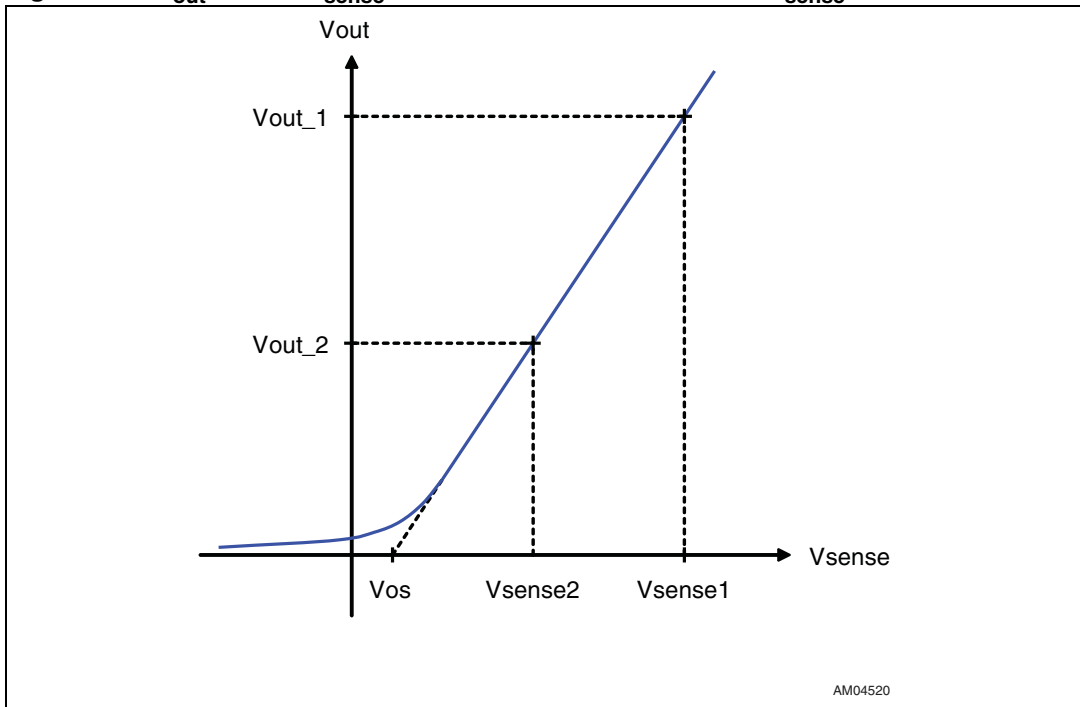
$$\text{SVR} = -20 \cdot \log \frac{\Delta V_{\text{out}}}{\Delta V_{CC} \cdot A_v}$$

5.3 Gain (A_v) and input offset voltage (V_{os})

The input offset voltage is defined as the intersection between the linear regression of the V_{out} vs. V_{sense} curve with the X-axis (see [Figure 17](#)). If V_{out1} is the output voltage with $V_{\text{sense}} = V_{\text{sense1}}$ and V_{out2} is the output voltage with $V_{\text{sense}} = V_{\text{sense2}}$, then V_{os} can be calculated with the following formula.

$$V_{os} = V_{\text{sense1}} - \left(\frac{V_{\text{sense1}} - V_{\text{sense2}}}{V_{\text{out1}} - V_{\text{out2}}} \cdot V_{\text{out1}} \right)$$

Figure 17. V_{out} versus V_{sense} characteristics: detail for low V_{sense} values



The values of V_{sense1} and V_{sense2} used for the input offset calculations are detailed in [Table 9](#).

Table 9. Test conditions for V_{os} voltage calculation

| A_v (V/V) | V_{sense1} (mV) | V_{sense2} (mV) |
|-------------|-------------------|-------------------|
| 20 | 50 | 5 |
| 25 | 50 | 5 |
| 50 | 50 | 5 |
| 100 | 40 | 5 |

5.4 Output voltage drift versus temperature

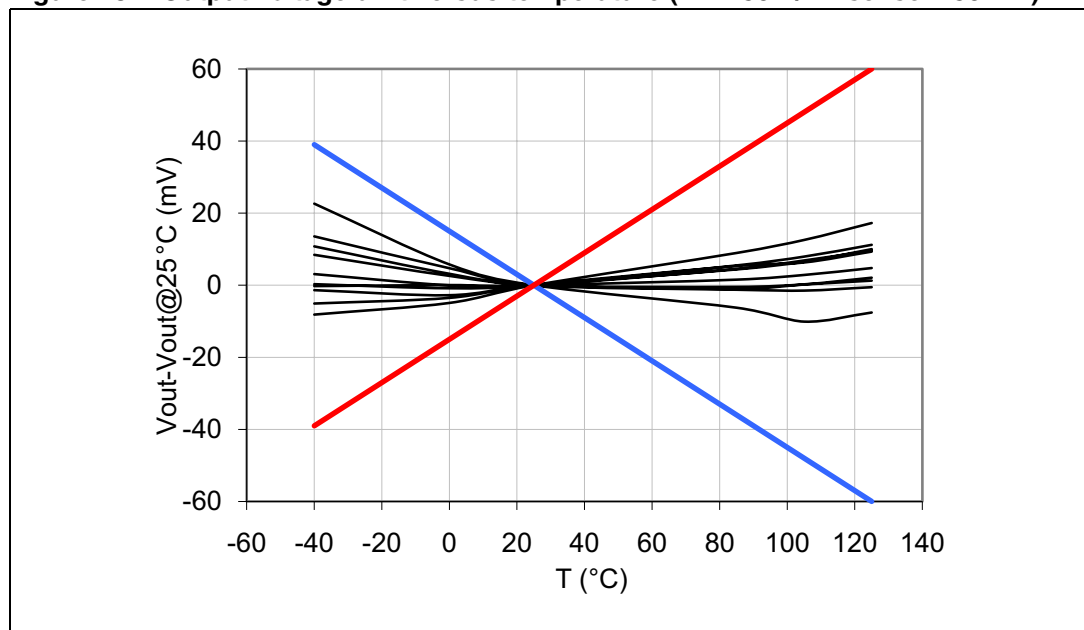
The output voltage drift versus temperature is defined as the maximum variation of V_{out} with respect to its value at 25° C over the temperature range. It is calculated as follows:

$$\frac{\Delta V_{out}}{\Delta T} = \max \frac{V_{out}(T_{amb}) - V_{out}(25^{\circ}C)}{T_{amb} - 25^{\circ}C}$$

with $T_{min} < T_{amb} < T_{max}$.

Figure 18 provides a graphical definition of the output voltage drift versus temperature. On this chart V_{out} is always within the area defined by the maximum and minimum variation of V_{out} versus T , and $T = 25^{\circ}C$ is considered to be the reference.

Figure 18. Output voltage drift versus temperature ($A_v = 50 V/V$ $V_{sense} = 50 mV$)



5.5 Input offset drift versus temperature

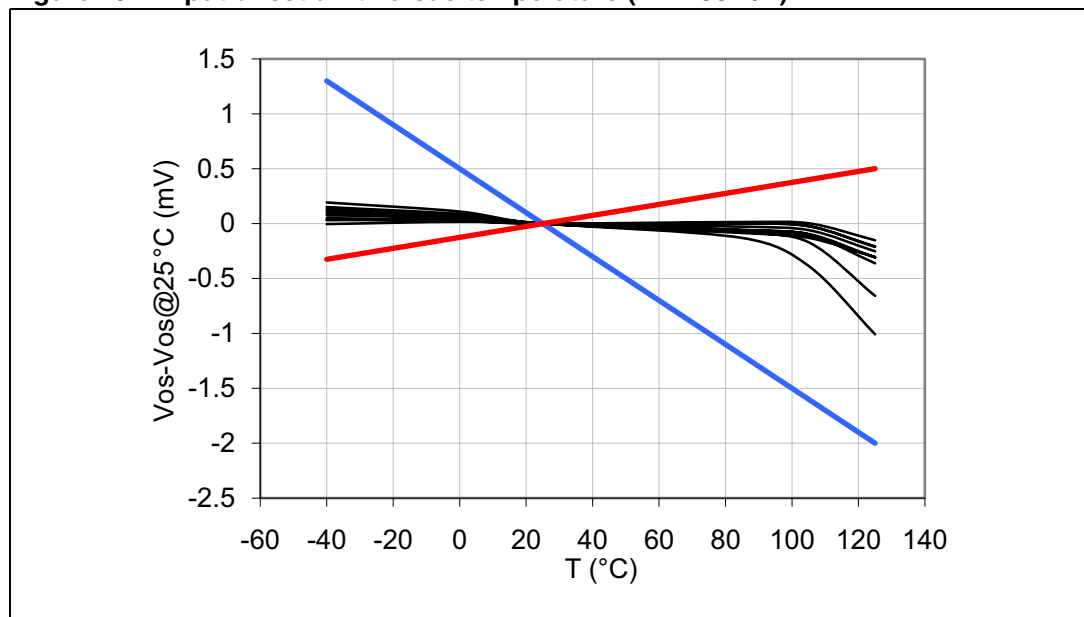
The input voltage drift versus temperature is defined as the maximum variation of V_{os} with respect to its value at 25° C over the temperature range. It is calculated as follows:

$$\frac{\Delta V_{os}}{\Delta T} = \max \frac{V_{os}(T_{amb}) - V_{os}(25^\circ C)}{T_{amb} - 25^\circ C}$$

with $T_{min} < T_{amb} < T_{max}$.

Figure 19. provides a graphical definition of the input offset drift versus temperature. On this chart V_{os} is always comprised in the area defined by the maximum and minimum variation of V_{os} versus T, and $T = 25^\circ C$ is considered to be the reference.

Figure 19. Input offset drift versus temperature ($A_v = 50 V/V$)



5.6 Output voltage accuracy

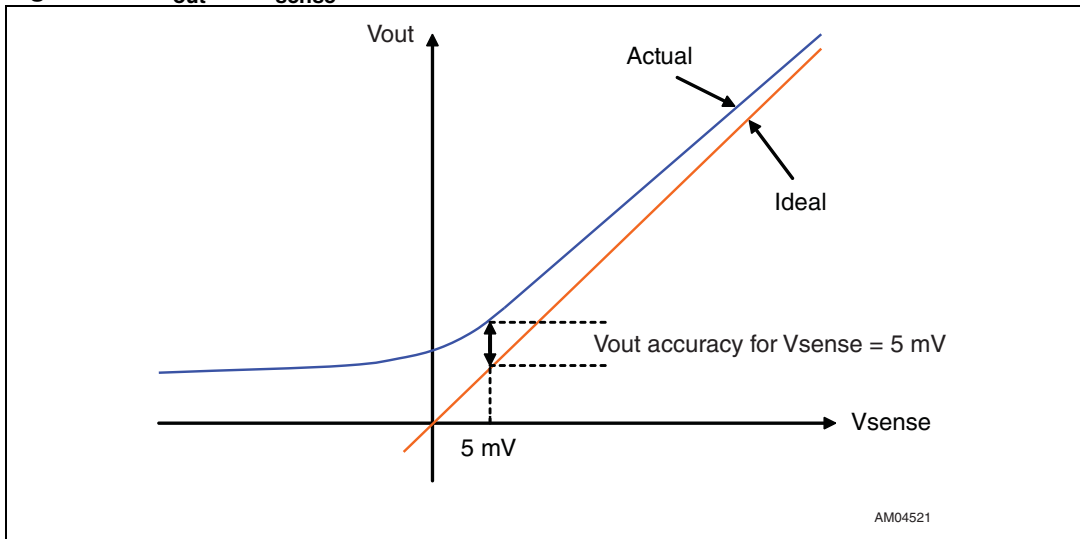
The output voltage accuracy is the difference between the actual output voltage and the theoretical output voltage. Ideally, the current sensing output voltage should be equal to the input differential voltage multiplied by the theoretical gain, as in the following formula.

$$V_{out-th} = A_v \cdot V_{sense}$$

The actual value is very slightly different, mainly due to the effects of:

- the input offset voltage V_{os} ,
- the non-linearity.

Figure 20. V_{out} vs. V_{sense} theoretical and actual characteristics



The output voltage accuracy, expressed as a percentage, can be calculated with the following formula,

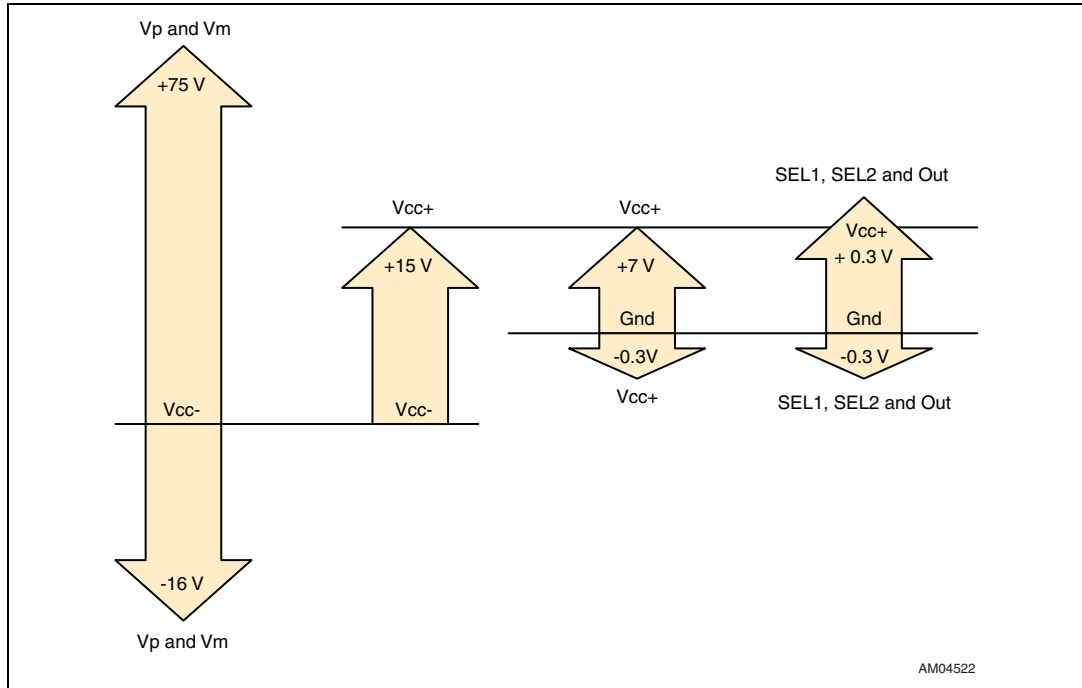
$$\Delta V_{out} = \frac{\text{abs}(V_{out} - (A_v \cdot V_{sense}))}{A_v \cdot V_{sense}}$$

with 20 V/V, 25 V/V, 50 V/V or 100 V/V depending on the configuration of the SEL1 and SEL2 pins.

6 Maximum permissible voltages on pins

The TSC103 can be used in either a single or dual supply configuration. The dual-supply configuration is achieved by disconnecting Vcc- and Gnd, and connecting Vcc- to a negative supply. *Figure 21* illustrates how the absolute maximum voltages on input pins Vp and Vm are referred to the Vcc- potential, while the maximum voltages on the positive supply pin, gain selection pins and output pins are referred to the Gnd pin. It should also be noted that the maximum voltage between Vcc- and Vcc+ is limited to 15 V.

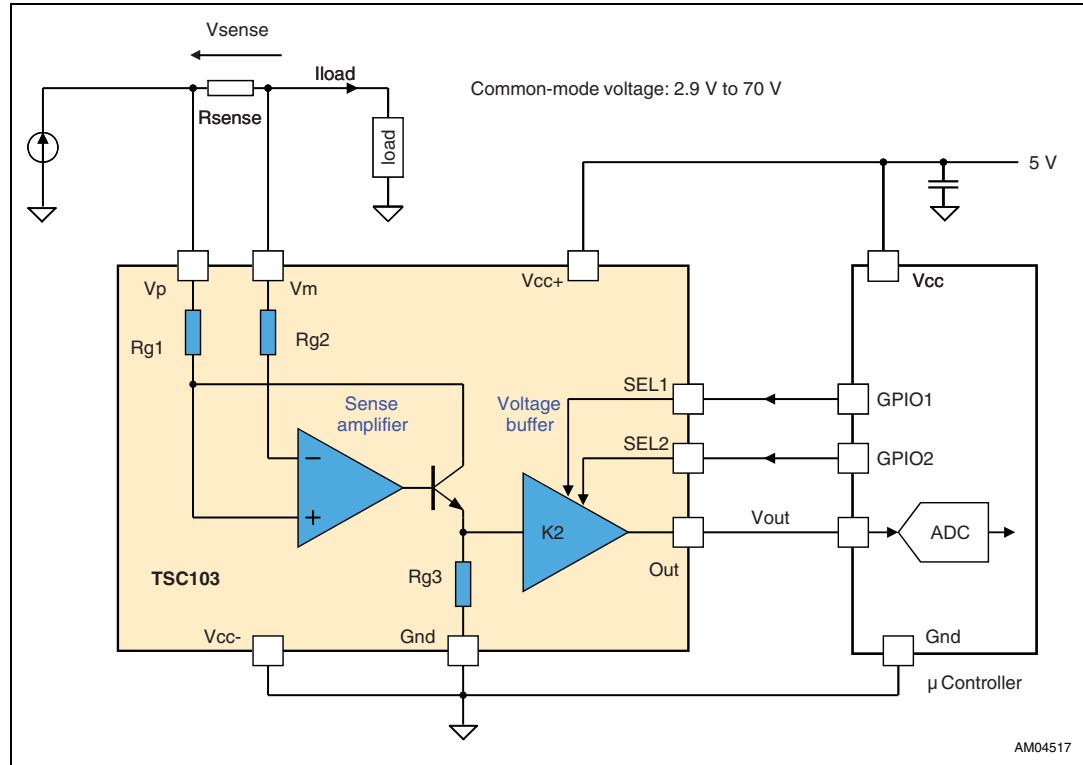
Figure 21. Maximum voltages on pins



7 Application information

The TSC103 can be used to measure current and to feed back the information to a microcontroller.

Figure 22. Single-supply configuration schematic



The current from the supply flows to the load through the R_{sense} resistor, causing a voltage drop equal to V_{sense} across R_{sense} . The amplifier's input currents are negligible, therefore its inverting input voltage is equal to V_m . The amplifier's open-loop gain forces its non-inverting input to the same voltage as the inverting input. As a consequence, the amplifier adjusts current flowing through R_{g1} so that the voltage drop across R_{g1} matches V_{sense} exactly.

Therefore, the drop across R_{g1} is:

$$V_{R_{g1}} = V_{sense} = R_{sense} \cdot I_{load}$$

If $I_{R_{g1}}$ is the current flowing through R_{g1} , then $I_{R_{g1}}$ is given by the formula:

$$I_{R_{g1}} = V_{sense} / R_{g1}$$

The $I_{R_{g1}}$ current flows entirely into resistor R_{g3} (the input bias current of the buffer is negligible). Therefore, the voltage drop on the R_{g3} resistor can be calculated as follows.

$$V_{R_{g3}} = R_{g3} \cdot I_{R_{g1}} = (R_{g3} / R_{g1}) \cdot V_{sense} = K1 \cdot V_{sense} \text{ with } K1 = R_{g3} / R_{g1}.$$

The voltage across the R_{g3} resistor is buffered to the Out pin by the voltage buffer, featuring a gain equal to $K2$. Therefore V_{out} can be expressed as:

$$V_{out} = K1 \cdot K2 \cdot V_{sense} = A_v \cdot V_{sense} \text{ with } A_v = K1 \cdot K2$$

or: $V_{out} = A_v \cdot R_{sense} \cdot I_{load}$

The resistor ratio $K1 = R_{g3}/R_{g1}$ is internally set to 20 V/V, and the voltage buffer gain K2 can be set to 1, 1.25, 2.5 or 5 depending on the voltage applied on SEL1 and SEL2 pins. Since they define the full-scale output range of the application, the R_{sense} resistor and the amplification gain A_v are important parameters and must therefore be selected carefully.

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

8.1 SO-8 package information

Figure 23. SO-8 package mechanical drawing

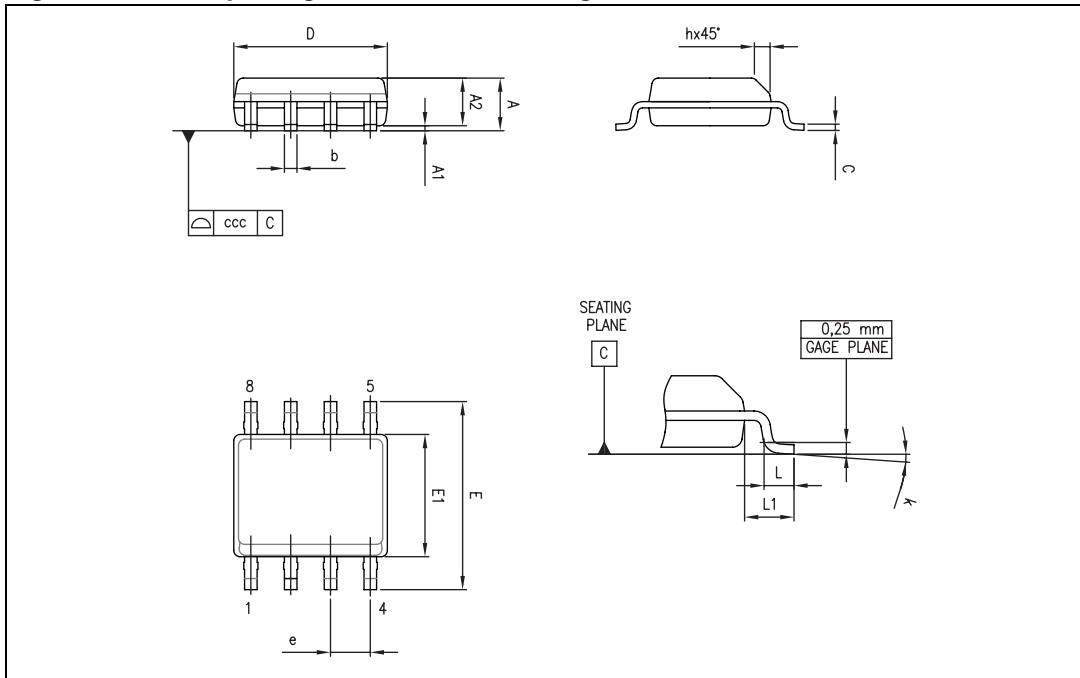


Table 10. SO-8 package mechanical data

| Ref. | Dimensions | | | | | |
|------|-------------|------|------|--------|-------|-------|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | | | 1.75 | | | 0.069 |
| A1 | 0.10 | | 0.25 | 0.004 | | 0.010 |
| A2 | 1.25 | | | 0.049 | | |
| b | 0.28 | | 0.48 | 0.011 | | 0.019 |
| c | 0.17 | | 0.23 | 0.007 | | 0.010 |
| D | 4.80 | 4.90 | 5.00 | 0.189 | 0.193 | 0.197 |
| E | 5.80 | 6.00 | 6.20 | 0.228 | 0.236 | 0.244 |
| E1 | 3.80 | 3.90 | 4.00 | 0.150 | 0.154 | 0.157 |
| e | | 1.27 | | | 0.050 | |
| h | 0.25 | | 0.50 | 0.010 | | 0.020 |
| L | 0.40 | | 1.27 | 0.016 | | 0.050 |
| L1 | | 1.04 | | | 0.040 | |
| k | 0 | | 8° | 1° | | 8° |
| ccc | | | 0.10 | | | 0.004 |

8.2 TSSOP-8 package information

Figure 24. TSSOP8 package mechanical drawing

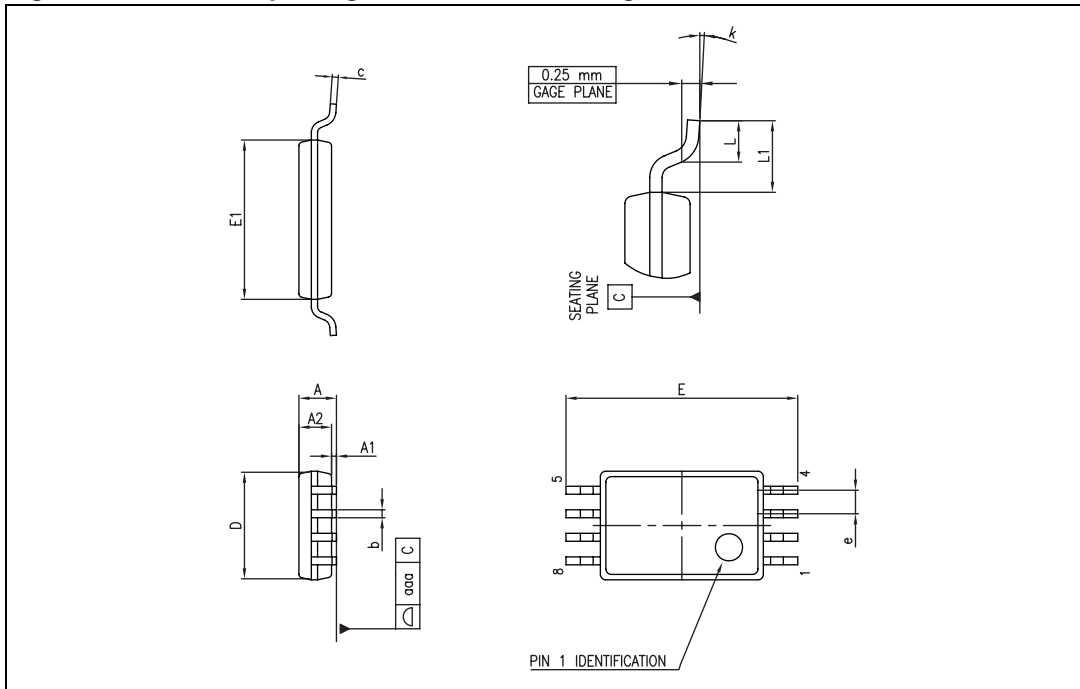


Table 11. TSSOP8 package mechanical data

| Ref. | Dimensions | | | | | |
|------|-------------|------|------|--------|--------|-------|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | | | 1.20 | | | 0.047 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.006 |
| A2 | 0.80 | 1.00 | 1.05 | 0.031 | 0.039 | 0.041 |
| b | 0.19 | | 0.30 | 0.007 | | 0.012 |
| c | 0.09 | | 0.20 | 0.004 | | 0.008 |
| D | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| E | 6.20 | 6.40 | 6.60 | 0.244 | 0.252 | 0.260 |
| E1 | 4.30 | 4.40 | 4.50 | 0.169 | 0.173 | 0.177 |
| e | | 0.65 | | | 0.0256 | |
| k | 0° | | 8° | 0° | | 8° |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | | 1 | | | 0.039 | |
| aaa | | | 0.10 | | | 0.004 |

9 Ordering information

Table 12. Order codes

| Part number | Temperature range | Package | Packaging | Marking |
|---------------------------|-------------------------------------|---------|-------------|---------|
| TSC103IPT | -40° C, +125° C | TSSOP8 | Tape & reel | 103I |
| TSC103IDT | | SO-8 | Tape & reel | TSC103I |
| TSC103IYPT ⁽¹⁾ | -40° C, +125° C Automotive grade | TSSOP8 | Tape & reel | 103Y |
| TSC103IYDT ⁽²⁾ | | SO-8 | Tape & reel | TSC103Y |

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent are on-going.
2. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.

10 Revision history

Table 13. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 04-Jan-2010 | 1 | Initial release. |
| 18-Nov-2011 | 2 | Added <i>Chapter 4: Electrical characteristics curves: current sense amplifier</i> . Changed <i>Figure 4</i> to <i>Figure 16</i> . Added automotive grade qualification for SO-8 package in <i>Table 12: Order codes</i> . |

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