

MOS FIELD EFFECT TRANSISTOR 2SJ598

SWITCHING P-CHANNEL POWER MOS FET

DESCRIPTION

The 2SJ598 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

• Low on-state resistance:

 $R_{DS(on)1} = 130 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = -10 \text{ V}, \text{ ID} = -6 \text{ A)}$

 $R_{DS(on)2} = 190 \text{ m}\Omega \text{ MAX.}$ (Vgs = -4.0 V, ID = -6 A)

- Low Ciss: Ciss = 720 pF TYP.
- Built-in gate protection diode
- TO-251/TO-252 package

ORDERING INFORMATION

PART NUMBER	PACKAGE			
2SJ598	TO-251 (MP-3)			
2SJ598-Z	TO-252 (MP-3Z)			

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (Vgs = 0 V)	VDSS	-60	V
Gate to Source Voltage (Vps = 0 V)	Vgss	∓20	V
Drain Current (DC) (Tc = 25°C)	I _{D(DC)}	Α	
Drain Current (pulse) Note1	D(pulse)	∓30	Α
Total Power Dissipation (Tc = 25°C)	PT	23	W
Total Power Dissipation (T _A = 25°C)	PT	1.0	W
Channel Temperature	T_ch	150	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Single Avalanche Current Note2	IAS	-12	Α
Single Avalanche Energy Note2	Eas	14.4	mJ

(TO-251)



(TO-252)



Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

2. Starting T_{ch} = 25°C, V_{DD} = -30 V, R_G = 25 Ω , V_{GS} = -20 \rightarrow 0 V

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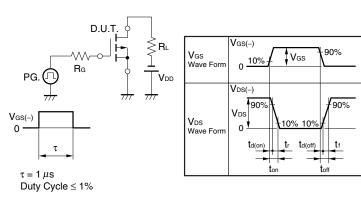
ELECTRICAL CHARACTERISTICS (TA = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	Vps = -60 V, Vgs = 0 V			-10	μΑ
Gate Leakage Current	Igss	V _{GS} = ∓16 V, V _{DS} = 0 V			∓10	μΑ
Gate Cut-off Voltage	V _{GS(off)}	$V_{DS} = -10 \text{ V}, I_{D} = -1 \text{ mA}$	-1.5	-2.0	-2.5	٧
Forward Transfer Admittance	yfs	V _{DS} = -10 V, I _D = -6 A	5	11		S
Drain to Source On-state Resistance	RDS(on)1	Vgs = -10 V, ID = -6 A		102	130	mΩ
	RDS(on)2	Vgs = -4.0 V, ID = -6 A		131	190	mΩ
Input Capacitance	Ciss	Vps = -10 V		720		pF
Output Capacitance	Coss	Vgs = 0 V		150		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		50		pF
Turn-on Delay Time	t d(on)	ID = -6 A		7		ns
Rise Time	t r	V _{GS} = -10 V		4		ns
Turn-off Delay Time	td(off)	V _{DD} = -30 V		35		ns
Fall Time	t f	$R_G = 0 \Omega$		10		ns
Total Gate Charge	Q _G	I _D = -12 A		15		nC
Gate to Source Charge	Qgs	V _{DD} = -48 V		3		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = -10 V		4		nC
Body Diode Forward Voltage	V _{F(S-D)}	IF = 12 A, VGS = 0 V		0.98		٧
Reverse Recovery Time	trr	IF = 12 A, VGS = 0 V		50		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A /μs		100		nC

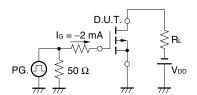
TEST CIRCUIT 1 AVALANCHE CAPABILITY

$V_{GS} = -20 \rightarrow 0 \text{ V}$ V_{DD} V_{DD}

TEST CIRCUIT 2 SWITCHING TIME

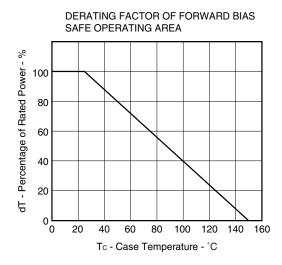


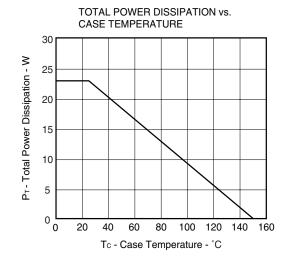
TEST CIRCUIT 3 GATE CHARGE



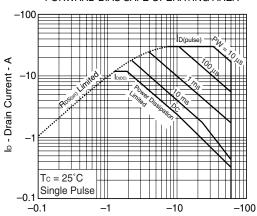


TYPICAL CHARACTERISTICS (TA = 25°C)



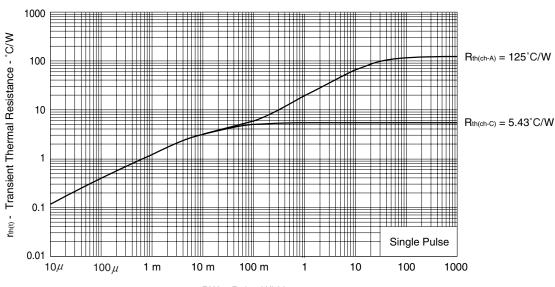


FORWARD BIAS SAFE OPERATING AREA



 $V_{\text{\scriptsize DS}}$ - Drain to Source Voltage - V

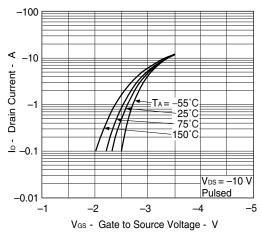
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

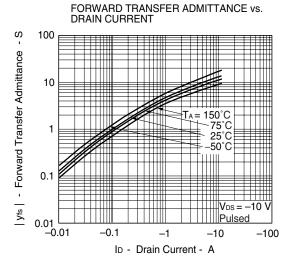


PW - Pulse Width - s

3

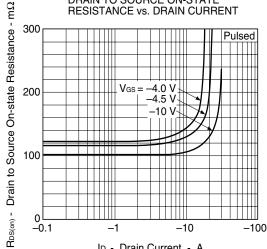
FORWARD TRANSFER CHARACTERISTICS





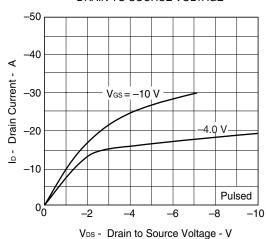
RESISTANCE vs. DRAIN CURRENT 300

DRAIN TO SOURCE ON-STATE

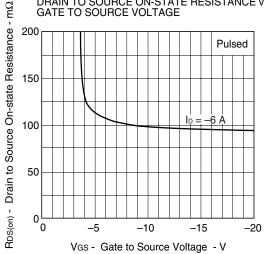


ID - Drain Current - A

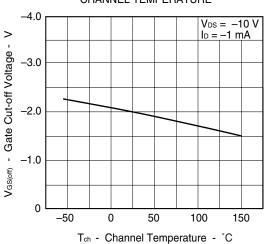
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

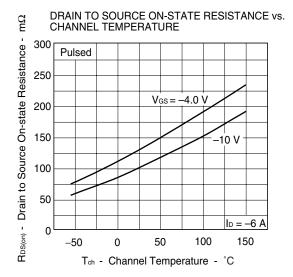


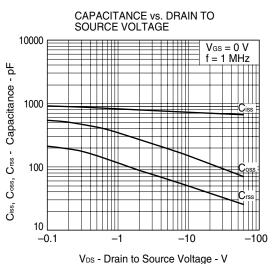
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE

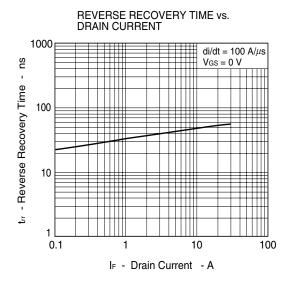


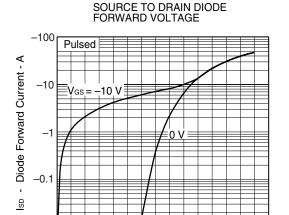
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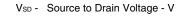










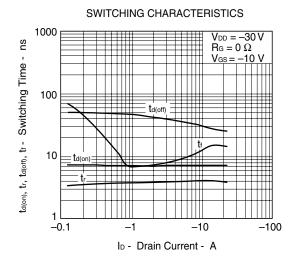


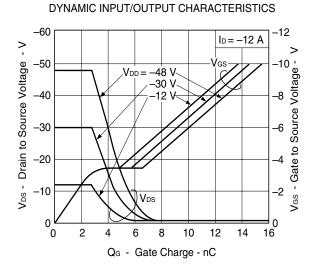
-1.0

-1.5

-0.5

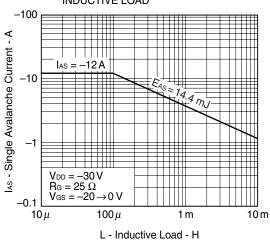
-0.01 L



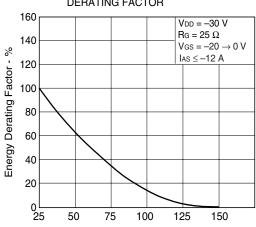


5

SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



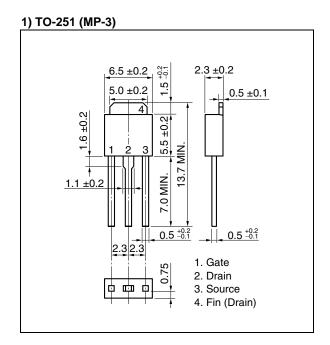
SINGLE AVALANCHE ENERGY DERATING FACTOR

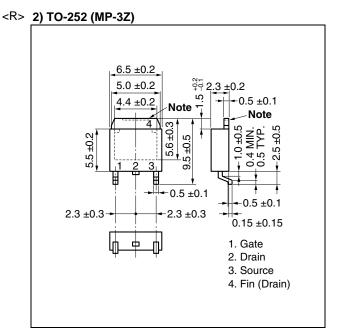


Starting Tch - Starting Channel Temperature - °C



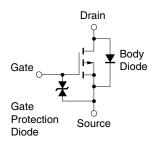
PACKAGE DRAWINGS (Unit: mm)





Note The depth of notch at the top of the fin is from 0 to 0.2 mm.

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD.

When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Data Sheet D14656EJ5V0DS 7

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