

## Japanese Equivalent JFET Types

### Silicon Junction Field-Effect Transistors

		Japanese	2SK17	2SK40	2SK59	2SK105
		InterFET	IFN17	IFN40	IFN59	IFN105
		Process	NJ16	NJ16	NJ16	NJ16
Parameters	Conditions	Unit Limit	N Channel	N Channel	N Channel	N Channel
$BV_{GSS}$	$I_G = -1.0 \mu A$	V Min	-20	-50	-30	-50
$I_{GSS}$	$V_{GS} = ()$ , $V_{DS} = \emptyset$	nA Max	0.10 (-10 V)	1.0 (-30 V)	1.0 (-10 V)	1.0 (-30 V)
$V_{GS(off)}$	$V_{DS} = ()$ , $I_D = 1.0 \text{ nA}$	V Min/Max	-0.5/-6.0 (10 V)	-0.4/-5.0 (15 V)	-0.4/-5.0 (10 V)	-0.25/-4.5 (5.0 V)
$I_{DSS}$	$V_{DS} = ()$ , $V_{GS} = \emptyset$	mA Min/Max	0.3/6.5 (10 V)	0.6/6.5 (15 V)	0.3/1.4 (10 V)	0.5/12 (5.0 V)
$g_{fs}$	$V_{DS} = ()$ , $V_{GS} = \emptyset$	mS Typ	2.0 (10 V)	2.0 (15 V)	1.5 (10 V)	2.1 (5.0 V)
$C_{iss}$	$V_{GS} = ()$ , $V_{DS} = ()$	pF Typ	4.0 ( $\emptyset$ ) ( $\emptyset$ )	4.0 ( $\emptyset$ ) (15 V)		4.0 ( $\emptyset$ ) (10 V)
$C_{rss}$	$V_{GS} = ()$ , $V_{DS} = ()$	pF Typ	1.2 (-10 V) ( $\emptyset$ )	1.2 ( $\emptyset$ ) (15 V)		1.0 ( $\emptyset$ ) (10 V)
Package Configuration			TO-226AA	TO-226AA	TO-226AA	TO-226AA
Pin Configuration			SGD	SGD	SGD	DGS