TOSHIBA FIELD EFFECT TRANSISTOR SILICON N CHANNEL MOS TYPE (L^2-π-MOSⅤ)

2SK2615

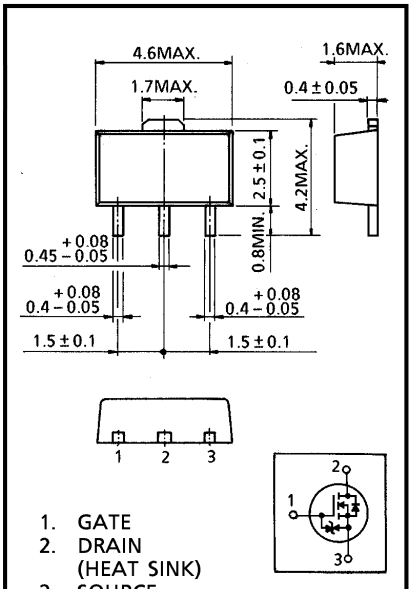
HIGH SPEED, HIGH CURRENT SWITCHING APPLICATIONS

DC-DC CONVERTER, RELAY DRIVE AND MOTOR DRIVE APPLICATIONS

INDUSTRIAL APPLICATIONS

- Low Drain-Source ON Resistance : $R_{DS\,(ON)}$ = 0.23Ω (Typ.)
- High Forward Transfer Admittance : $|Y_{fs}|$ = 2.0S (Typ.)
- Low Leakage Current : I_{DSS} = 100μA (Max.) (V_{DS} = 60V)
- Enhancement-Mode : V_{th} = 0.8~2.0V (V_{DS} = 10V, I_D = 1mA)

Unit in mm



JEDEC	—
EIAJ	—
TOSHIBA	2-5K1B

Weight : 0.05g (Typ.)

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Drain-Source Voltage		V_{DSS}	60	V
Drain-Gate Voltage (R_{GS} = 20kΩ)		V_{DGR}	60	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current	DC	I_D	2	A
	Pulse	I_{DP}	6	
Drain Power Dissipation (Ta = 25°C)		P_D	0.5	W
Drain Power Dissipation		P_D*	1.5	W
Channel Temperature		T_{ch}	150	°C
Storage Temperature Range		T_{stg}	−55~150	°C

* : Mounted on ceramic substrate (600mm² × 0.8t)

MARKING

THERMAL CHARACTERISTICS

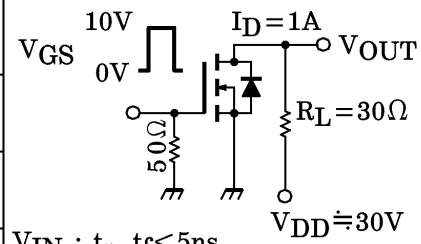
CHARACTERISTIC	SYMBOL	MAX.	UNIT
Thermal Resistance, Channel to Ambient	$R_{th\,(ch\text{-}a)}$	250	°C / W

This transistor is an electrostatic sensitive device.
Please handle with caution.

961001EAA2

- TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

ELECTRICAL CHARACTERISTICS (Ta = 25°C)

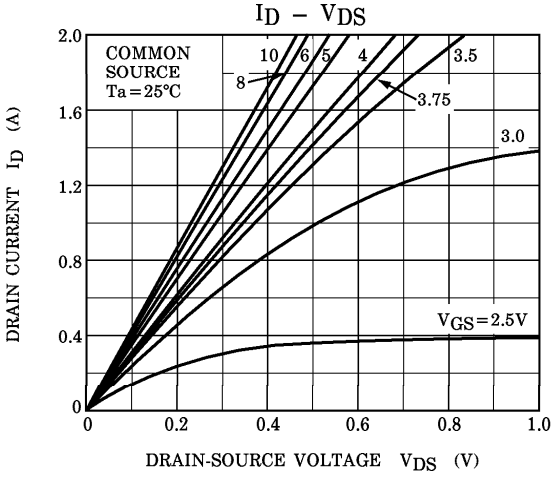
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gate Leakage Current		I_{GSS}	$V_{GS}=\pm16V$, $V_{DS}=0V$	—	—	±10	μA
Drain Cut-off Current		I_{DSS}	$V_{DS}=60V$, $V_{GS}=0V$	—	—	100	μA
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	$I_D=10mA$, $V_{GS}=0V$	60	—	—	V
Gate Threshold Voltage		V_{th}	$V_{DS}=10V$, $I_D=1mA$	0.8	—	2.0	V
Drain-Source ON Resistance		$R_{DS(ON)}$	$V_{GS}=4V$, $I_D=1A$	—	0.33	0.44	Ω
			$V_{GS}=10V$, $I_D=1A$	—	0.23	0.30	
Forward Transfer Admittance		$\|Y_{fs}\|$	$V_{DS}=10V$, $I_D=1A$	1.0	2.0	—	S
Input Capacitance		C_{iss}	$V_{DS}=10V$, $V_{GS}=0V$, f=1MHz	—	150	—	pF
Reverse Transfer Capacitance		C_{rss}		—	25	—	
Output Capacitance		C_{oss}		—	70	—	
Switching Time	Rise Time	t_r		—	25	—	ns
	Turn-on Time	t_{on}		—	30	—	
	Fall Time	t_f		—	50	—	
	Turn-off Time	t_{off}		—	150	—	
Total Gate Charge (Gate-Source Plus Gate-Drain)		Q_g	$V_{DD}\fallingdotseq48V$, $V_{GS}=10V$, $I_D=2A$	—	6.0	—	nC
Gate-Source Charge		Q_{gs}		—	4.6	—	
Gate-Drain ("Miller") Charge		Q_{gd}		—	1.4	—	

V_{IN} : t_r, $t_f<5ns$,
Duty ≦ 1%, $t_w=10\mu s$

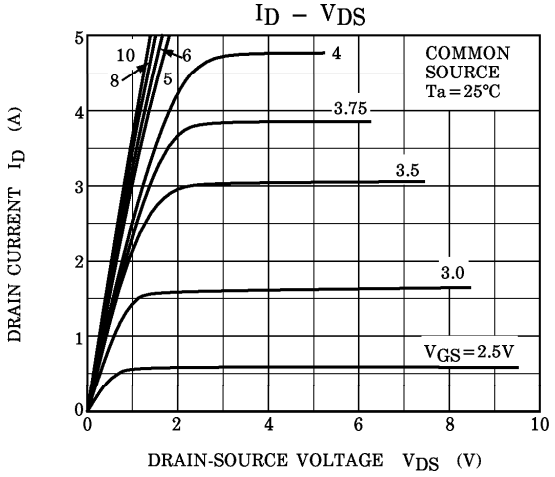
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Continuous Drain Reverse Current	I_{DR}	—	—	—	2	A
Pulse Drain Reverse Current	I_{DRP}	—	—	—	6	A
Diode Forward Voltage	V_{DSF}	$I_{DR}=2A$, $V_{GS}=0V$	—	—	−1.5	V
Reverse Recovery Time	t_{rr}	$I_{DR}=2A$, $V_{GS}=0V$	—	100	—	ns
Reverse Recovered Charge	Q_{rr}	$dI_{DR}/dt=50A/\mu s$	—	40	—	μC

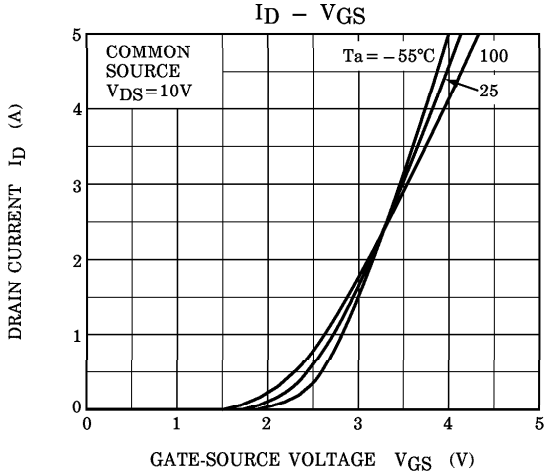
$I_D - V_{DS}$



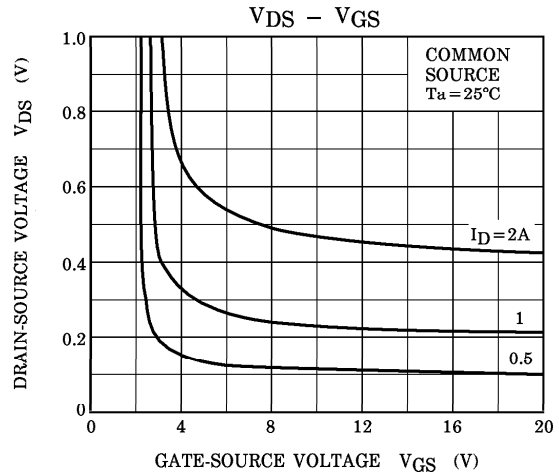
$I_D - V_{DS}$



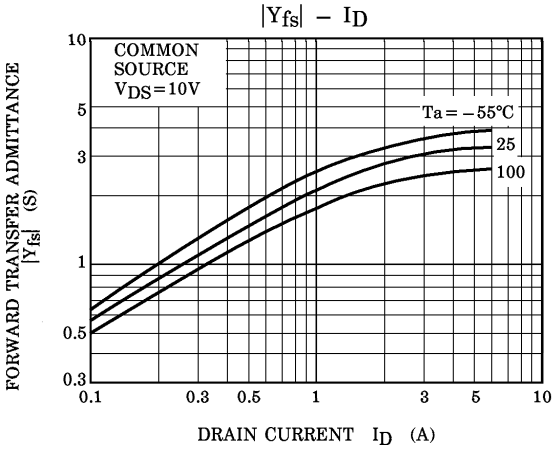
$I_D - V_{GS}$



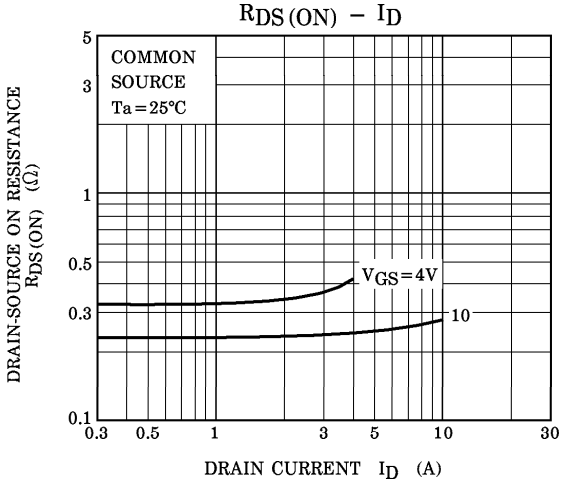
$V_{DS} - V_{GS}$



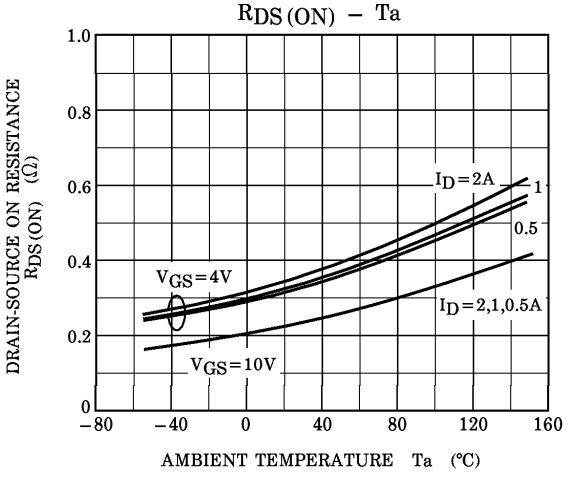
$|Y_{fs}| - I_D$



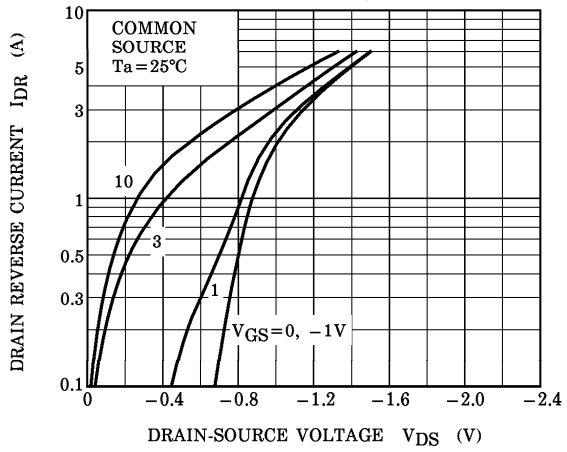
$R_{DS(ON)} - I_D$



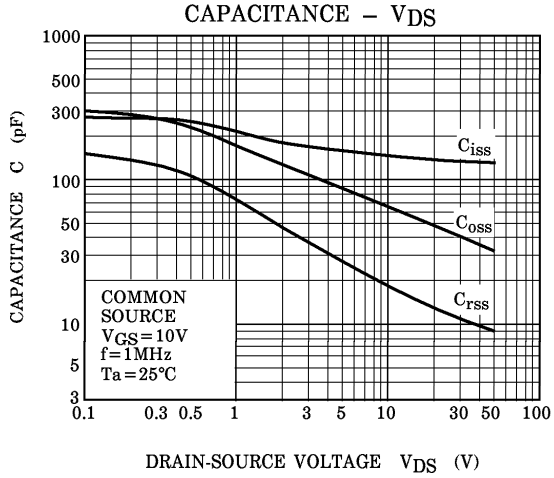
$R_{DS\,(ON)}$ – Ta



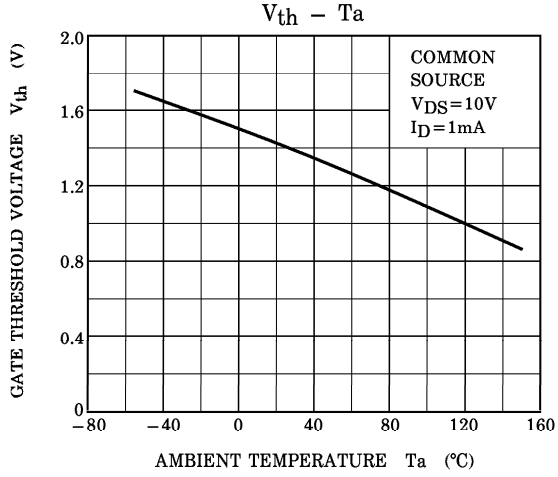
I_{DR} – V_{DS}



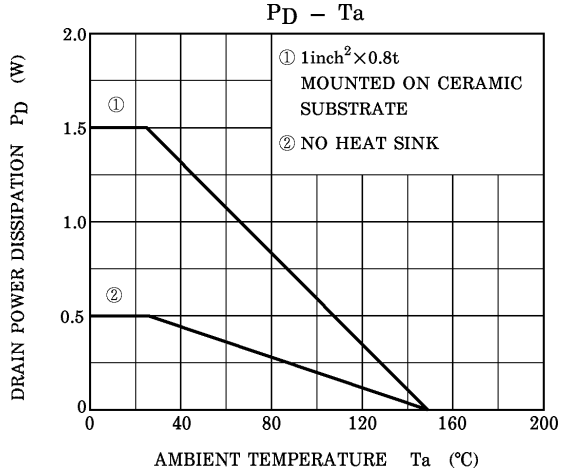
CAPACITANCE – V_{DS}



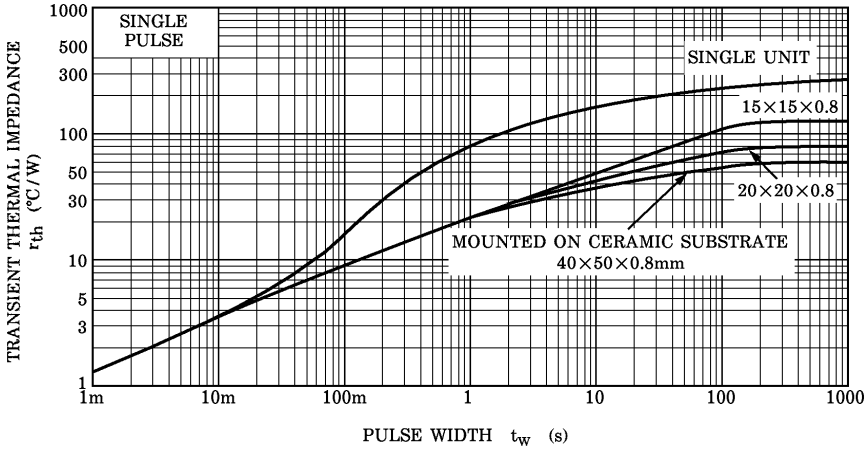
V_{th} – Ta



P_D – Ta



r_{th} – t_w



SAFE OPERATING AREA