International
IOR Rectifier

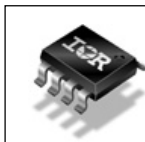
PD- 93844B

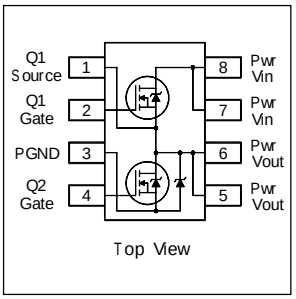
IRF7901D1

- Co-Pack Dual N-channel HEXFET® Power MOSFET and Schottky Diode
- Ideal for Synchronous Buck DC-DC Converters Up to 5A Peak Output
- Low Conduction Losses
- Low Switching Losses
- Low Vf Schottky Rectifier

Dual FETKY™

Co-Packaged Dual MOSFET Plus Schottky Diode


SO-8



Device Ratings (Max.Values)

	Q1	Q2 and Schottky
V_{DS}	30V	30V
$R_{DS(on)}$	38 mΩ	32 mΩ
Q_G	10.5 nC	18.3 nC
Q_{sw}	3.8 nC	9.0 nC
V_{SD}	1.0V	0.52V

Description

The FETKY™ family of Co-Pack HEXFET®MOSFETs and Schottky diodes offers the designer an innovative, board space saving solution for switching regulator and power management applications. Advanced HEXFET®MOSFETs combined with low forward drop Schottky results in an extremely efficient device suitable for a wide variety of portable electronics applications.

The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. Internal connections enable easier board layout design with reduced stray inductance.

Absolute Maximum Ratings

Parameter		Symbol	IRF7901D1	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Output Current ($V_{GS} \geq 4.5V$)④	T_L = 100°C	I_D	6.2	A
Pulsed Drain Current①		I_{DM}	24	
Power Dissipation③	T_L = 100°C	P_D	2.0	W
Junction & Storage Temperature Range		T_J, T_{STG}	–55 to 150	°C
Pulsed Source Current ①		I_{SM}	12	A

Thermal Resistance

Parameter		Max.	Units
Maximum Junction-to-Ambient③	$R_{\theta JA}$	62.5	°C/W
Maximum Junction-to-Lead⑤	$R_{\theta JL}$	25	°C/W

9/19/01

Electrical Characteristics

		Q1 - Control FET			Q2 - Synch FET & Schottky				
Parameter		**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Drain-to-Source Breakdown Voltage*	BV_{DSS}	30	–	–	30	–	–	V	V_{GS} = 0V, I_D = 250µA
Static Drain-Source on Resistance*	R_{DS}(on)	–	28	38	–	23	32	mΩ	V_{GS} = 4.5V, I_D = 5A②
Gate Threshold Voltage*	V_{GS}(th)	1.0	–	–	1.0	–	–	V	V_{DS} = V_{GS}, I_D = 250µA
Drain-Source Leakage	I_{DSS}	–	–	30	–	–	30	µA	V_{DS} = 24V, V_{GS} = 0
		–	–	0.15	–	–	4.3	mA	V_{DS} = 24V, V_{GS} = 0, T_J = 125°C
Gate-Source Leakage Current*	I_{GSS}	–	–	±100	–	–	±100	nA	V_{GS} = ±20V
Total Gate Charge*	$Q_{G\ cont}$	–	7.6	10.5	–	15.5	21.0		V_{GS} = 5V, V_{DS} = 16V, I_D = 5A
	$Q_{G\ synch}$	–	6.7	9.0	–	13.5	18.3		V_{GS} = 5V, V_{DS} = 100mV, I_D = 5A
Pre-Vth Gate-Source Charge	Q_{GS1}	–	2.0	–	–	5.5	–		V_{DS} = 16V, I_D = 5A
Post-Vth Gate-Source Charge	Q_{GS2}	–	0.5	–	–	0.9	–	nC	
Gate to Drain Charge	Q_{GD}	–	1.9	–	–	4.7	–		
Switch Charge* (Q_{gs2} + Q_{gd})	Q_{sw}	–	2.4	3.8	–	5.6	9.0		
Output Charge*	Q_{oss}	–	13.5	18.0	–	9.0	12.3		V_{DS} = 16V, V_{GS} = 0
Gate Resistance	R_G	–	3.4	–	–	4.3	–	Ω	
Input Capacitance	C_{iss}	–	780	–	–	1810	–		
Output Capacitance	C_{oss}	–	430	–	–	310	–	pF	V_{DS} = 16V, V_{GS} = 0, f = 1MHz
Transfer Capacitance	C_{rss}	–	30	–	–	110	–		
Turn-On Delay Time	t_d(on)	–	7.2	–	–	10.4	–		V_{DD} = 16V, I_D = 5A, V_{GS} = 5V
Rise Time	t_r	–	13.8	–	–	16.4	–	ns	Clamped inductive load
Turn-Off Delay Time	t_d(off)	–	14.7	–	–	14.6	–		See test diagram Fig 17.
Fall Time	t_f	–	8	–	–	5.2	–		

Source-Drain Ratings and Characteristics

		Q1			Q2 & parallel Schottky				
Parameter		**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Diode Forward Voltage*②	V_{SD}	–	0.7	1.0	–	0.48	0.52	V	I_S = 1A, V_{GS} = 0V
Reverse Recovery Charge	Q_{rr}	–	62.3	–	–	8.9	–	nC	dI/dt = 700A/us V_{DS} = 16V, V_{GS} = 0V, I_S = 5A

① Repetitive rating; pulse width limited by max. junction temperature.
② Pulse width ≤ 300 µs; duty cycle ≤ 2%.
③ When mounted on 1 inch square copper board, t < 10 sec.
④ Combined Q1, Q2 I_{RMS} @ Pwr V_{out} pins. Calculated continuous current based on maximum allowable junction temperature; switching or other losses will decrease RMS current capability
⑤ When mounted on IRNBPS2 design kit. Measured as device T_J to Pwr leads (V_{in} & V_{out})
* Devices are 100% tested to these parameters.

Power MOSFET Optimization for DC-DC Converters

Table 1 and Table 2 describes the event during the various charge segments and shows an approximation of losses during that period.

Table 1 – Control FET Losses

	Description	Segment Losses
Conduction Loss	Losses associated with MOSFET on time. I_{RMS} is a function of load current and duty cycle.	$P_{COND} = I_{RMS}^2 \times R_{DS(on)}$
Gate Drive Loss	Losses associated with charging and discharging the gate of the MOSFET every cycle. Use the control FET Q_G.	$P_{IN} = V_G \times Q_G \times f$
Switching Loss	Losses during the drain voltage and drain current transitions for every full cycle. Losses occur during the Q_{GS2} and Q_{GD} time period and can be simplified by using Q_{switch}.	$P_{QGS2} \approx V_{IN} \times I_L \times \frac{Q_{GS2}}{I_G} \times f$ $P_{QGD} \approx V_{IN} \times I_L \times \frac{Q_{GD}}{I_G} \times f$ $P_{SWITCH} \approx V_{IN} \times I_L \frac{Q_{SW}}{I_G} \times f$
Output Loss	Losses associated with the Q_{OSS} of the device every cycle when the control FET turns on. Losses are caused by both FETs, but are dissipated by the control FET.	$P_{OUTPUT} = \frac{Q_{OSS}}{2} \times V_{IN} \times f$

Table 2 – Synchronous FET Losses

	Description	Segment Losses
Conduction Loss	Losses associated with MOSFET on time. I_{RMS} is a function of load current and duty cycle.	$P_{COND} = I_{RMS}^2 \times R_{DSon}$
Gate Drive Loss	Losses associated with charging and discharging the gate of the MOSFET every cycle. Use the Sync FET Q_G.	$P_{IN} = V_G \times Q_G \times f$
Switching Loss	Generally small enough to ignore except at light loads when the current reverses in the output inductor. Under these conditions various light load power saving techniques are employed by the control IC to maintain switching losses to a negligible level.	$P_{SWITCH} \approx 0$ $P_{OUTPUT} = \frac{Q_{OSS}}{2} \times V_{IN} \times f$
Output Loss	Losses associated with the Q_{OSS} of the device every cycle when the control FET turns on. They are caused by the synchronous FET, but are dissipated in the control FET.	

Typical Application

The performance of the new Dual FETKY™ has been tested in-circuit using IR's new IRNBPS2 "Dual Output Synchronous Buck Design Kit", operating up to $21V_{in}$ and 5A peak output current, with operating voltages from $1V_{out}$ to $5V_{out}$.

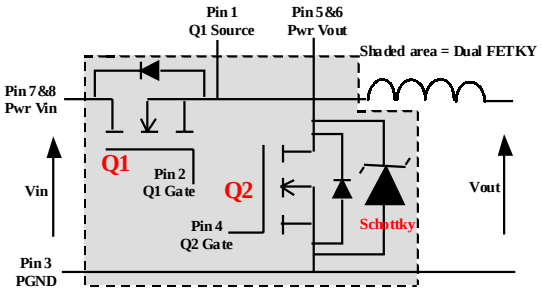


Figure 1: Synchronous Buck dc-dc Topology

Typical Application (Contd.)

The Dual FETKY integrates all the power semiconductor devices for DC-DC conversion within one SO-8 package, as shown on page 1. The high side control MOSFET (Q1) is optimized for low combined Q_{sw} and R_{DS}(on). The low side synchronous MOSFET (Q2) is optimized for low R_{DS}(on) and high Cdv/dt immunity. The ultra-low V_f schottky diode is internally connected in parallel with the synchronous MOSFET, for improved deadtime efficiency. For ease of circuit board layout, the Dual FETKY has been internally configured such that it represents a functional block for the power device portion of the synchronous buck DC-DC converter. This helps to minimize the external PCB traces compared to a discrete solution.

In-Circuit Efficiency

The in-circuit efficiency curves for the Dual FETKY are shown in Figure 2 & 3. The Dual FETKY can achieve up to 96.6% and 94.6% peak efficiency for the 5.0V and 3.3V applications respectively, with excellent maximum load efficiency.

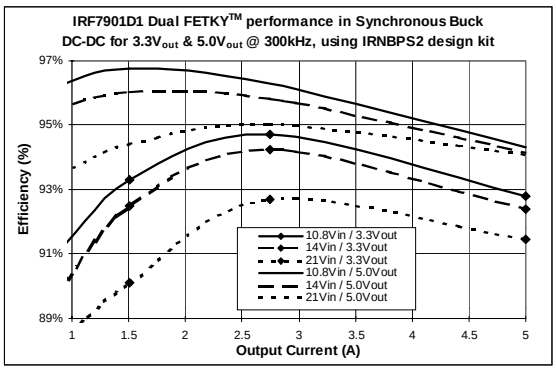


Figure 2. IRF7901D1 Dual FETKY™ electrical efficiency at 3.3Vout & 5.0Vout.

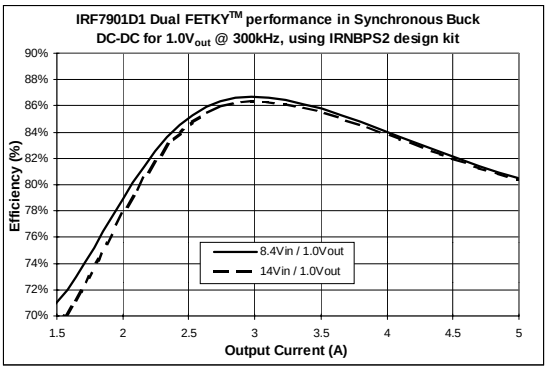


Figure 3. IRF7901D1 Dual FETKY™ electrical efficiency at 1.0Vout.

Typical Characteristics

Q1 - Control FET

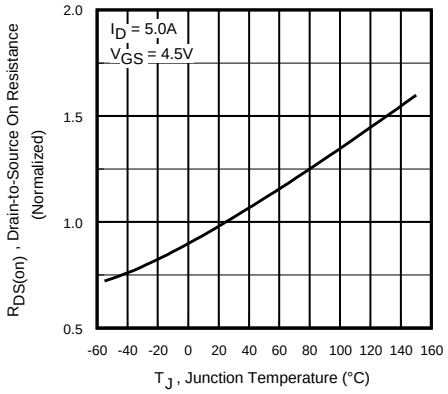


Figure 4. Normalized On-Resistance vs Junction Temperature

Q2 - Synchronous FET & Schottky

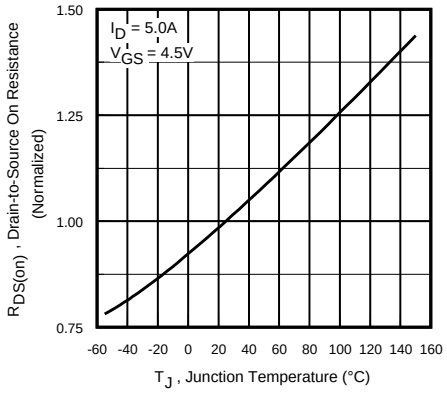


Figure 5. Normalized On-Resistance vs Junction Temperature

Typical Characteristics

Q1 - Control FET

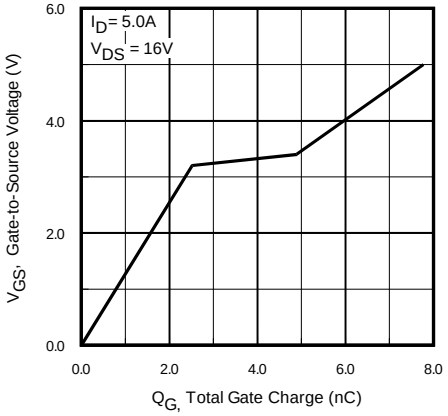


Figure 6. Gate-to-Source Voltage vs Typical Gate Charge

Q2 - Synchronous FET & Schottky

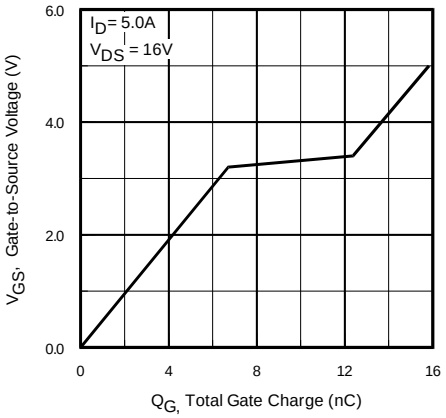


Figure 7. Gate-to-Source Voltage vs Typical Gate Charge

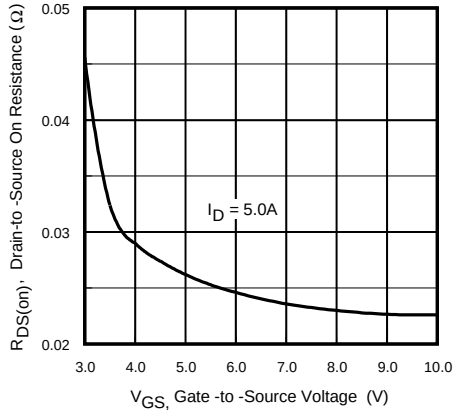


Figure 8. Typical R_{DS}(on) vs Gate-to-Source Voltage

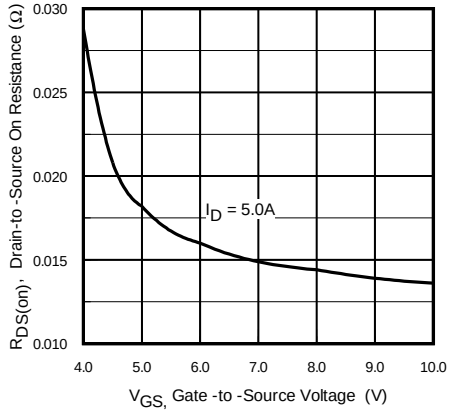


Figure 9. Typical R_{DS}(on) vs Gate-to-Source Voltage

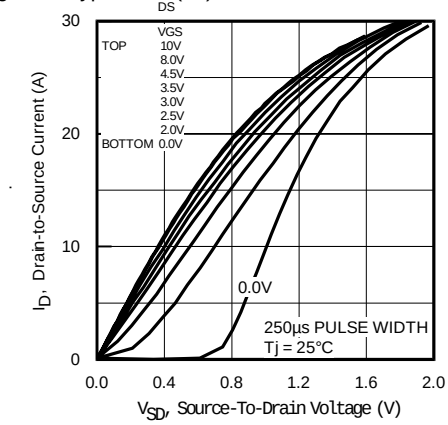


Figure 10. Typical Reverse Output Characteristics

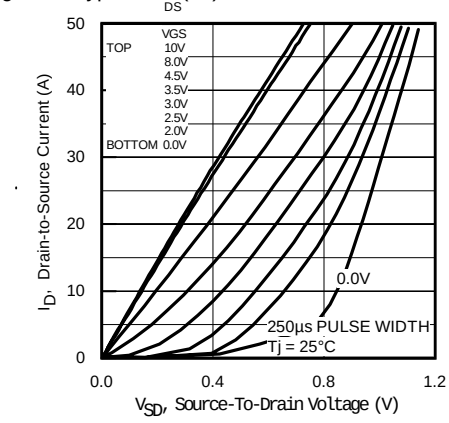


Figure 11. Typical Reverse Output Characteristics

Typical Characteristics

Q1 - Control FET

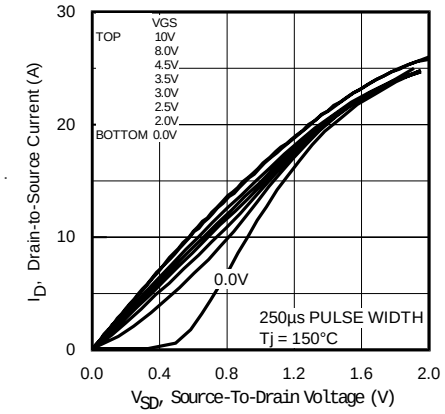


Figure 12. Typical Reverse Output Characteristics

Q2 - Synchronous FET & Schottky

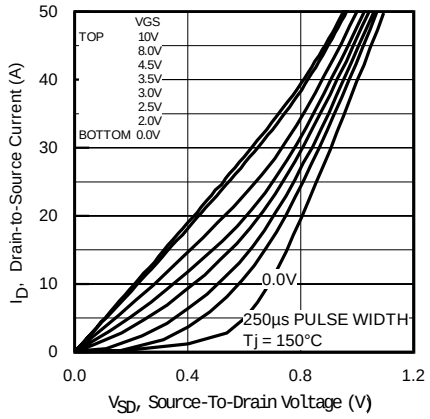


Figure 13. Typical Reverse Output Characteristics

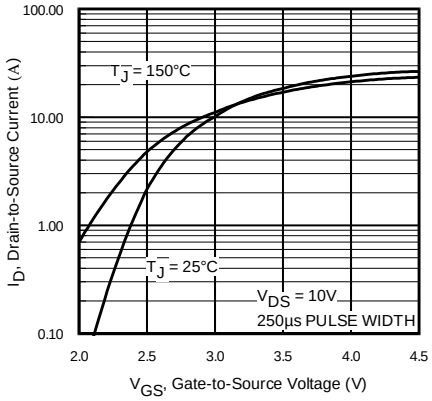


Figure 14. Typical Transfer Characteristic

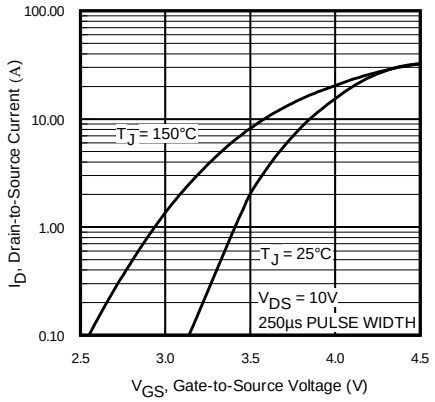


Figure 15. Typical Transfer Characteristic

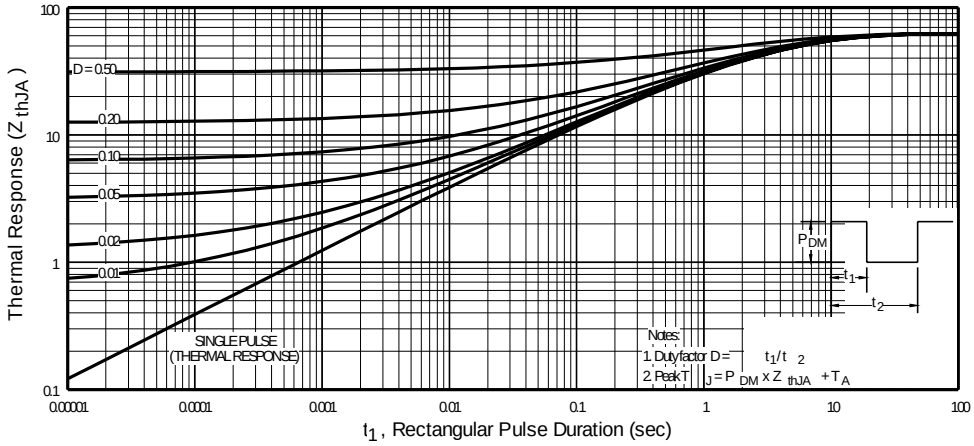


Figure 16. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

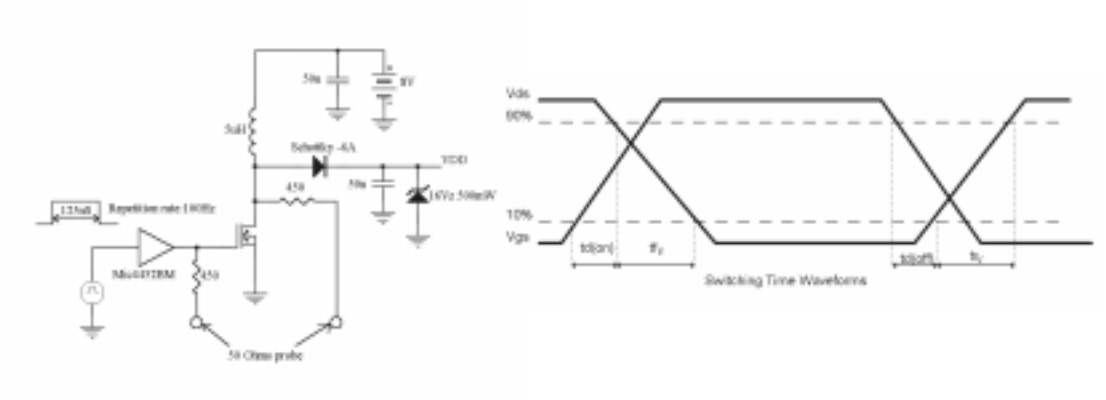
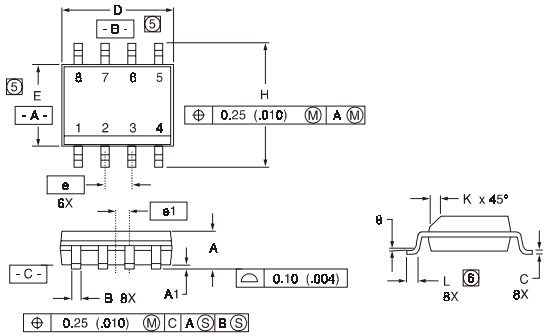


Figure 17. Clamped Inductive Load Test Diagram and Switching waveform.

SO-8 Package Outline

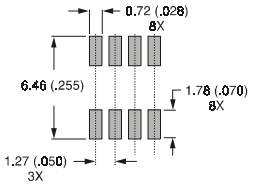


	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.014	.018	0.36	0.46
C	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.16	.050	0.41	1.27
θ	0°	8°	0°	8°

NOTES:

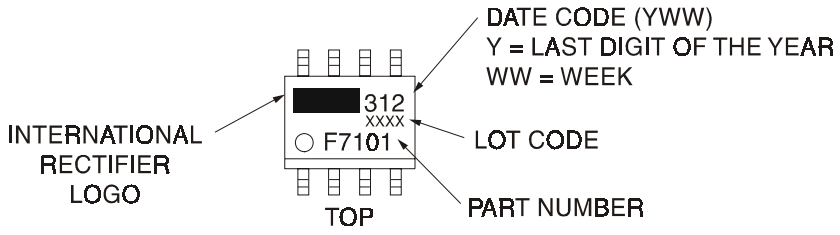
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.006).
6. DIMENSIONS IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE..

RECOMMENDED FOOTPRINT



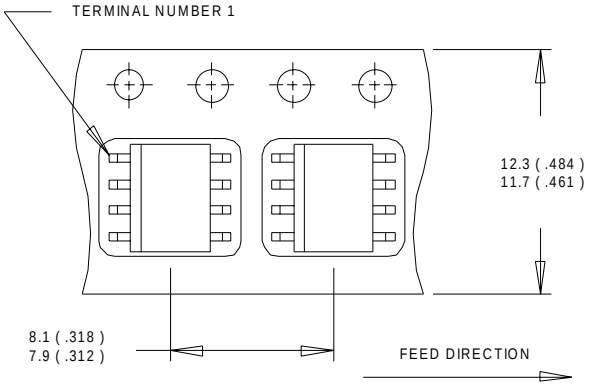
Part Marking Information

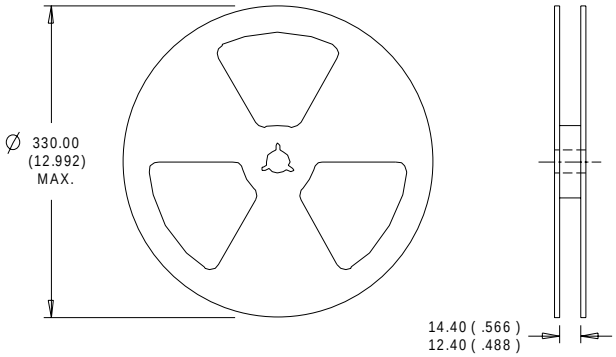
EXAMPLE: THIS IS AN IRF7101



SO-8 Tape & Reel Information

Dimensions are shown in millimeters (inches)





NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

International
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Data and specifications subject to change without notice.
This product has been designed and qualified for the consumer market.
Qualification Standards can be found on IR's Web site.

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