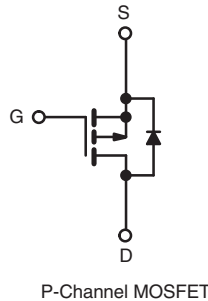
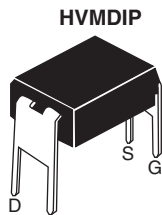


## Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	- 200	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = - 10$ V	3.0
$Q_g$ (Max.) (nC)	8.9	
$Q_{gs}$ (nC)	2.1	
$Q_{gd}$ (nC)	3.9	
Configuration	Single	



### FEATURES

- Dynamic  $dV/dt$  Rating
- Repetitive Avalanche Rated
- For Automatic Insertion
- End Stackable
- P-Channel
- Fast Switching
- Ease of Paralleling
- Compliant to RoHS Directive 2002/95/EC



### DESCRIPTION

The Power MOSFETs technology is the key to Vishay advanced line of Power MOSFET transistors. The efficient geometry and unique processing of the Power MOSFETs design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness. The 4 pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1" pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 W.

ORDERING INFORMATION	
Package	HVMDIP
Lead (Pb)-free	IRFD9210PbF SiHFD9210-E3
SnPb	IRFD9210 SiHFD9210

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	- 200	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$		
Continuous Drain Current	$V_{GS}$ at - 10 V	$T_A = 25$ °C	- 0.40	A
		$T_A = 100$ °C	- 0.25	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	- 3.2		
Linear Derating Factor		0.0083	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	210	mJ	
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	- 0.40	A	
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	0.10	mJ	
Maximum Power Dissipation	$T_A = 25$ °C	$P_D$	1.0	W
Peak Diode Recovery $dV/dt^c$		$dV/dt$	- 5.0	V/ns
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s		300 <sup>d</sup>	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = - 50$  V, starting  $T_J = 25$  °C,  $L = 123$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = - 1.6$  A (see fig. 12).
- $I_{SD} \leq - 2.3$  A,  $dI/dt \leq 70$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C.
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	120	°C/W

**SPECIFICATIONS** ( $T_J = 25\text{ °C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-200	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ °C}$ , $I_D = -1\text{ mA}$	-	-0.23	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-2.0	-	-4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -200\text{ V}, V_{GS} = 0\text{ V}$	-	-	-100	$\mu\text{A}$
		$V_{DS} = -160\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ °C}$	-	-	-500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -0.24\text{ A}^b$	-	-	3.0	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = -50\text{ V}, I_D = -0.24\text{ A}$	0.27	-	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V},$ $V_{DS} = -25\text{ V},$ $f = 1.0\text{ MHz}$ , see fig. 5	-	170	-	pF
Output Capacitance	$C_{oss}$		-	54	-	
Reverse Transfer Capacitance	$C_{rss}$		-	16	-	
Total Gate Charge	$Q_g$	$V_{GS} = -10\text{ V},$ $I_D = -1.3\text{ A}, V_{DS} = -160\text{ V}$ see fig. 6 and 13 <sup>b</sup>	-	-	8.9	nC
Gate-Source Charge	$Q_{gs}$		-	-	2.1	
Gate-Drain Charge	$Q_{gd}$		-	-	3.9	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -100\text{ V}, I_D = -2.3\text{ A}$ $R_g = 24\text{ }\Omega, R_D = 41\text{ }\Omega,$ see fig. 10 <sup>b</sup>	-	8.0	-	ns
Rise Time	$t_r$		-	12	-	
Turn-Off Delay Time	$t_{d(off)}$		-	11	-	
Fall Time	$t_f$		-	13	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact	-	4.0	-	nH
Internal Source Inductance	$L_S$		-	6.0	-	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode	-	-	-0.40	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	-3.2	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ °C}, I_S = -0.40\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	-5.8	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ °C}, I_F = -2.3\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$	-	110	220	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	0.56	1.1	$\mu\text{C}$

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

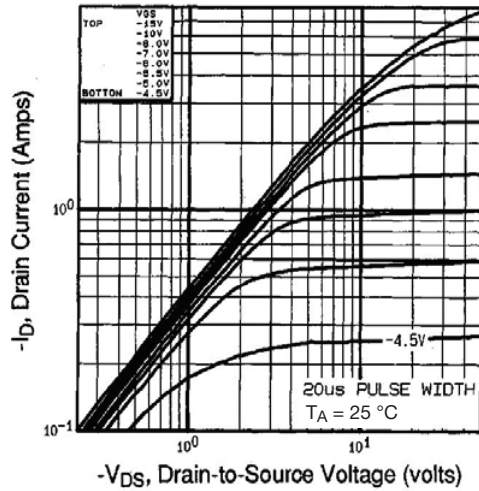


Fig. 1 - Typical Output Characteristics,  $T_A = 25\text{ °C}$

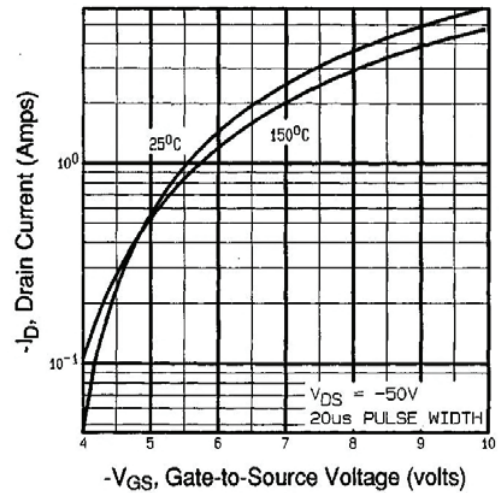


Fig. 3 - Typical Transfer Characteristics

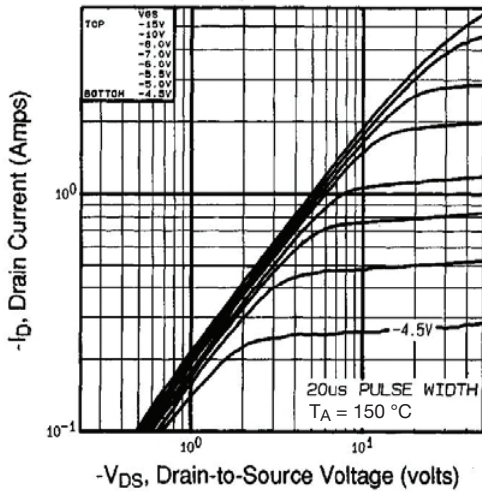


Fig. 2 - Typical Output Characteristics,  $T_A = 150\text{ °C}$

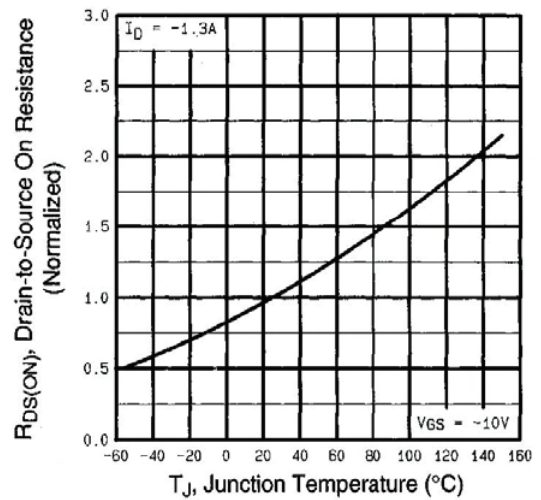


Fig. 4 - Normalized On-Resistance vs. Temperature

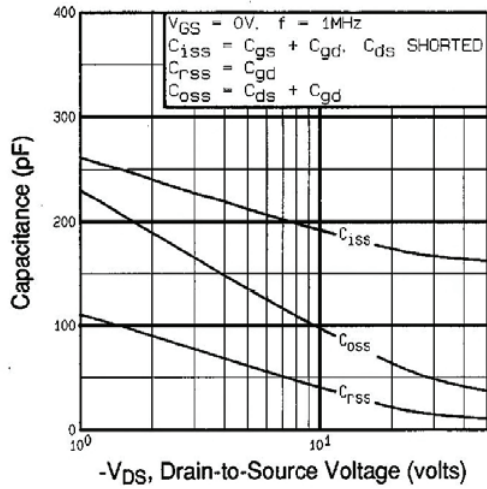


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

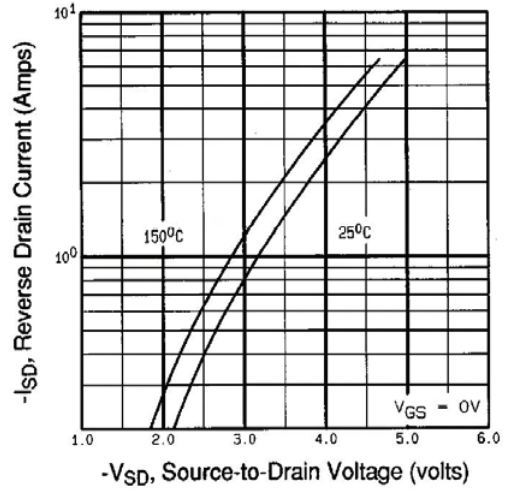


Fig. 7 - Typical Source-Drain Diode Forward Voltage

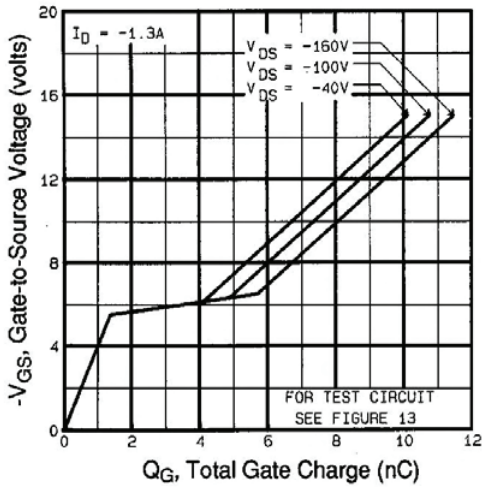


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

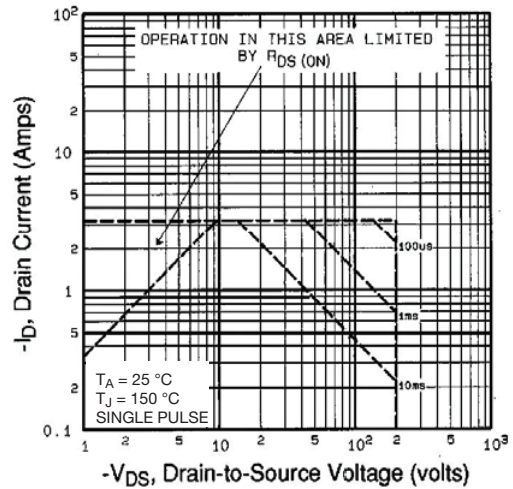
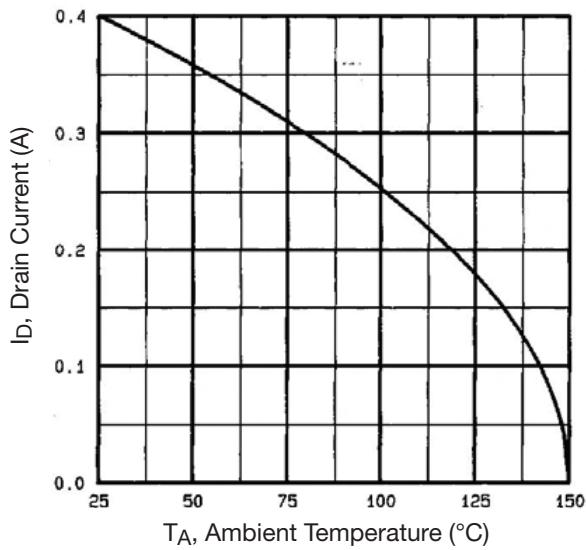
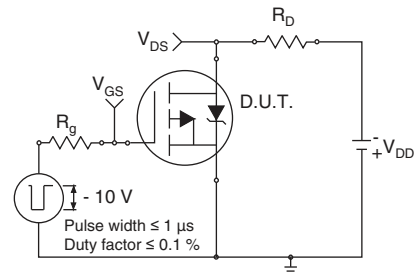


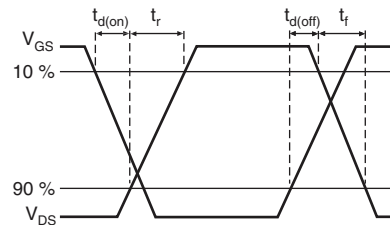
Fig. 8 - Maximum Safe Operating Area



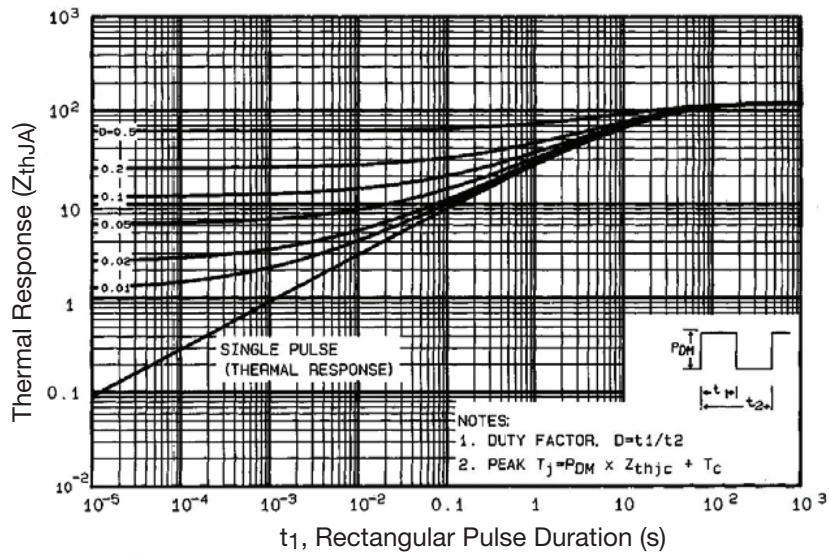
**Fig. 9 - Maximum Drain Current vs. Ambient Temperature**



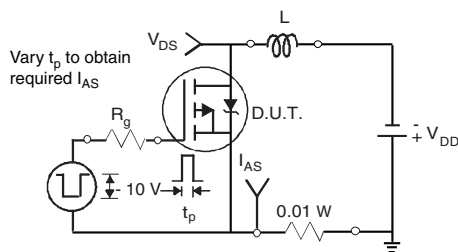
**Fig. 10a - Switching Time Test Circuit**



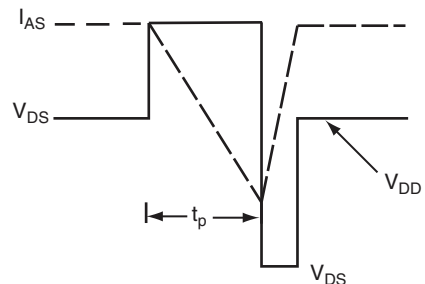
**Fig. 10b - Switching Time Waveforms**



**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient**



**Fig. 12a - Unclamped Inductive Test Circuit**



**Fig. 12b - Unclamped Inductive Waveforms**

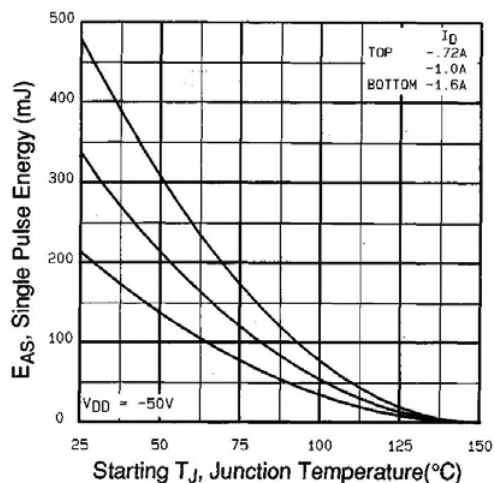


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

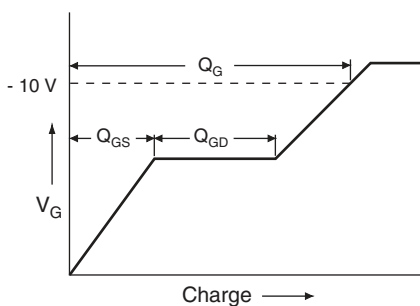


Fig. 13a - Basic Gate Charge Waveform

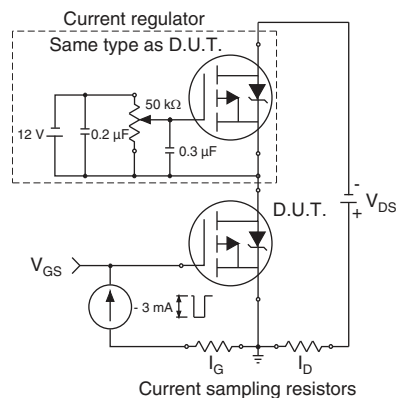
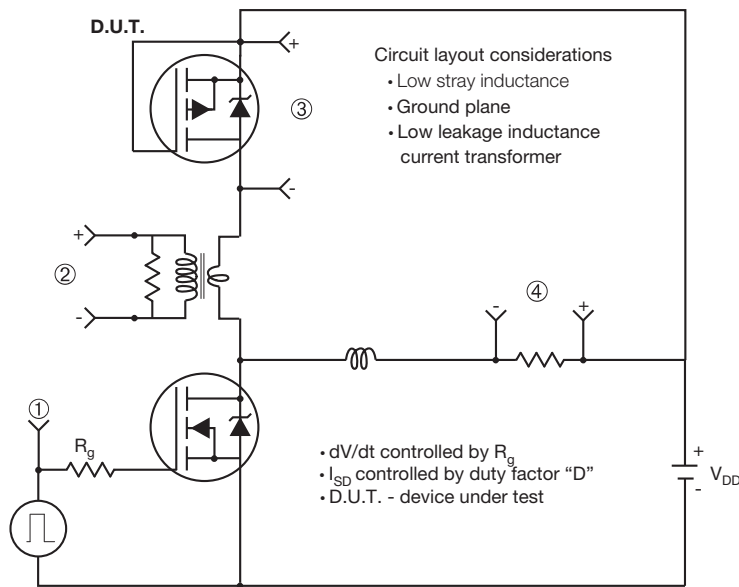
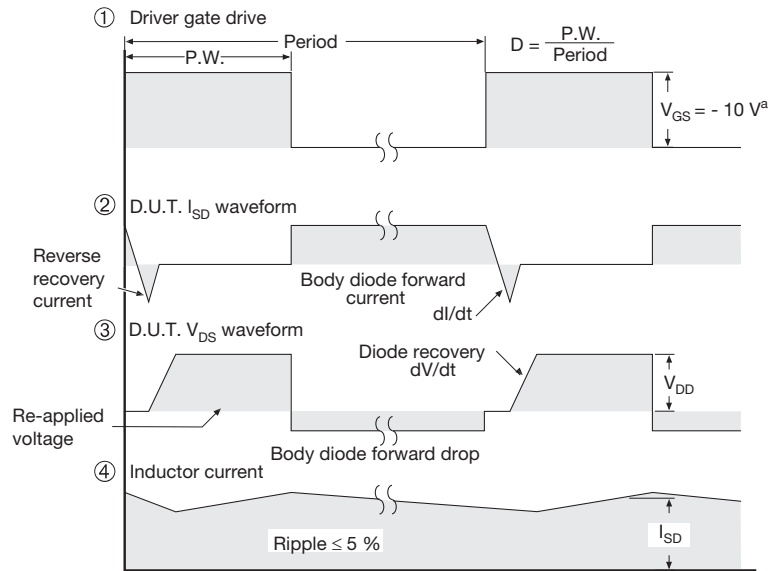


Fig. 13b - Gate Charge Test Circuit

### Peak Diode Recovery dV/dt Test Circuit



**Note**  
• Compliment N-Channel of D.U.T. for driver



**Note**  
a.  $V_{GS} = -5V$  for logic level and  $-3V$  drive devices

**Fig. 14 - For P-Channel**

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## HVM DIP (High voltage)



DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.310	0.330	7.87	8.38
E	0.300	0.425	7.62	10.79
L	0.270	0.290	6.86	7.36

ECN: X10-0386-Rev. B, 06-Sep-10  
DWG: 5974

### Note

- Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.





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