

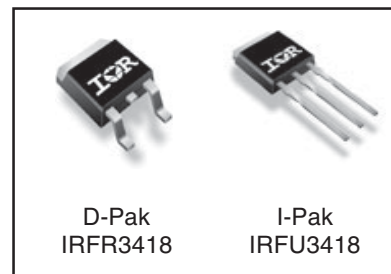
**Applications**

- High frequency DC-DC converters

<b>V<sub>DSS</sub></b>	<b>R<sub>DS(on)</sub> Max</b>	<b>I<sub>D</sub></b>
<b>80V</b>	<b>14mΩ</b>	<b>30A</b>

**Benefits**

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C<sub>OSS</sub> to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



**Absolute Maximum Ratings**

	Parameter	Max.	Units
V <sub>DS</sub>	Drain-to-Source Voltage	80	V
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	70 <sup>Ⓞ</sup>	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	50	
I <sub>DM</sub>	Pulsed Drain Current <sup>Ⓛ</sup>	280	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation	140	W
P <sub>D</sub> @ T <sub>A</sub> = 25°C	Maximum Power Dissipation	3.8	
	Linear Derating Factor	0.95	W/°C
dv/dt	Peak Diode Recovery dv/dt <sup>Ⓜ</sup>	5.2	V/ns
T <sub>J</sub>	Operating Junction and	-55 to + 175	°C
T <sub>STG</sub>	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case	—	1.05	°C/W
R <sub>θJA</sub>	Junction-to-Ambient (PCB Mount) *	—	40	
R <sub>θJA</sub>	Junction-to-Ambient	—	110	

Notes <sup>Ⓛ</sup> through <sup>Ⓞ</sup> are on page 10

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# IRFR/U3418

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Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	80	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.08	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	11.5	14	mΩ	$V_{GS} = 10V, I_D = 18A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.5	—	5.5	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 80V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 64V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$

Dynamic @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	66	—	—	S	$V_{DS} = 25V, I_D = 18A$
$Q_g$	Total Gate Charge	—	63	94	nC	$I_D = 18A$
$Q_{gs}$	Gate-to-Source Charge	—	23	—		$V_{DS} = 40V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	23	—		$V_{GS} = 10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	24	—	ns	$V_{DD} = 40V$
$t_r$	Rise Time	—	72	—		$I_D = 18A$
$t_{d(off)}$	Turn-Off Delay Time	—	41	—		$R_G = 6.8\Omega$
$t_f$	Fall Time	—	27	—		$V_{GS} = 10V$ ④
$C_{iss}$	Input Capacitance	—	3510	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	330	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	190	—		$f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	1220	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	240	—		$V_{GS} = 0V, V_{DS} = 64V, f = 1.0\text{MHz}$
$C_{oss\ eff.}$	Effective Output Capacitance	—	360	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 64V$ ③

## Avalanche Characteristics

	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy ②⑥	—	260	mJ
$I_{AR}$	Avalanche Current ①	—	18	A

## Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	70	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①⑥	—	—	280		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 18A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	57	—	ns	$T_J = 150^\circ\text{C}, I_F = 18A, V_{DD} = 25V$
$Q_{rr}$	Reverse Recovery Charge	—	130	—	nC	$di/dt = 100A/\mu s$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

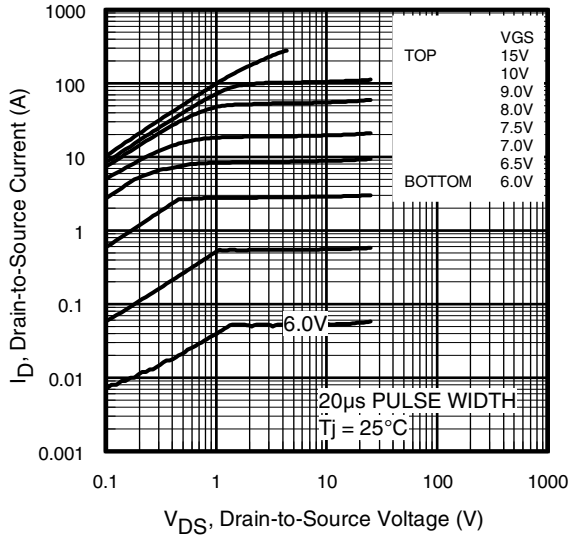


Fig 1. Typical Output Characteristics

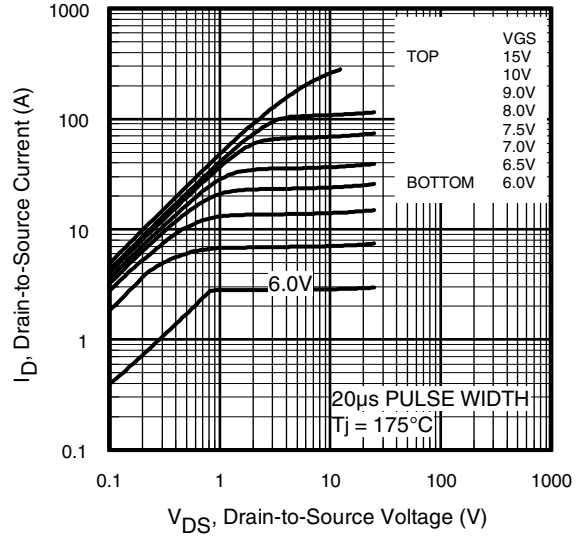


Fig 2. Typical Output Characteristics

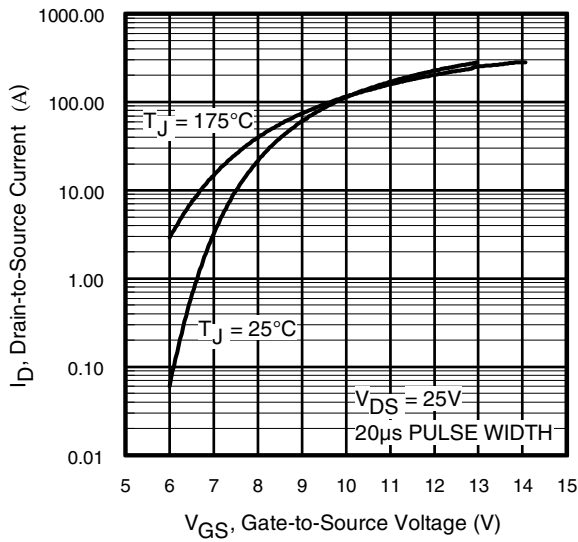


Fig 3. Typical Transfer Characteristics

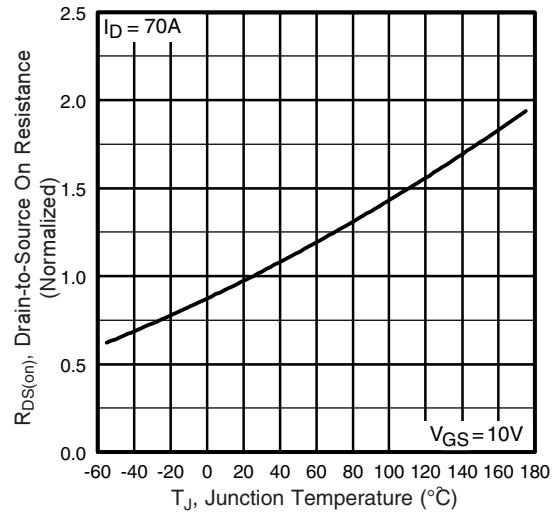
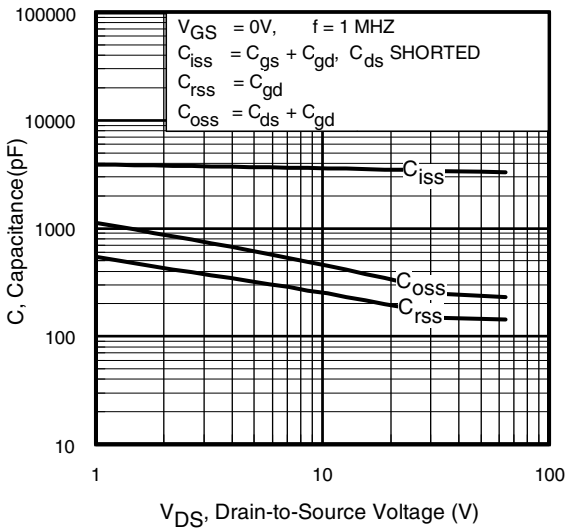
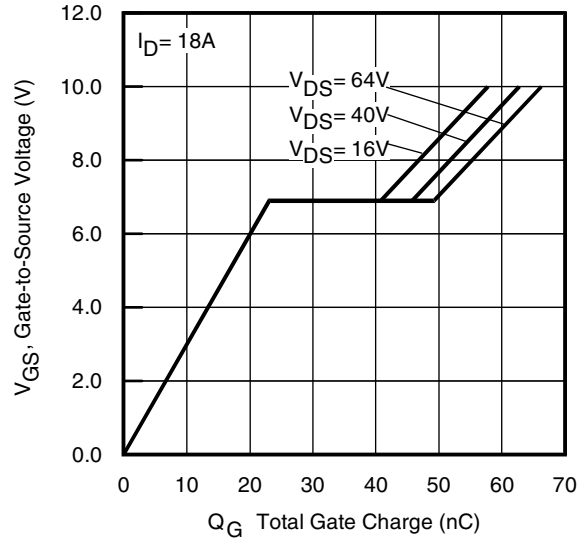


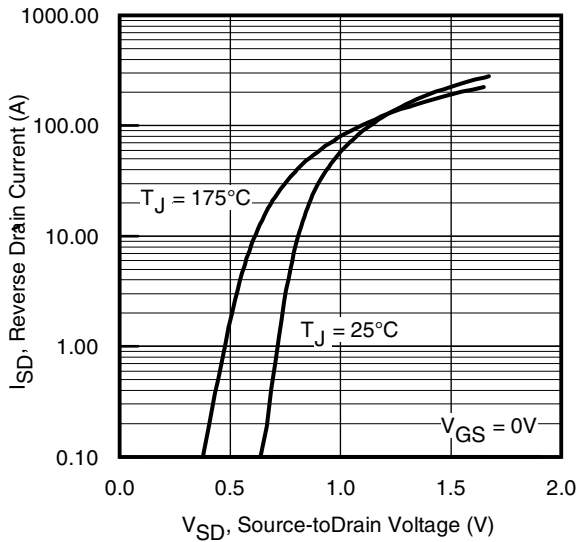
Fig 4. Normalized On-Resistance Vs. Temperature



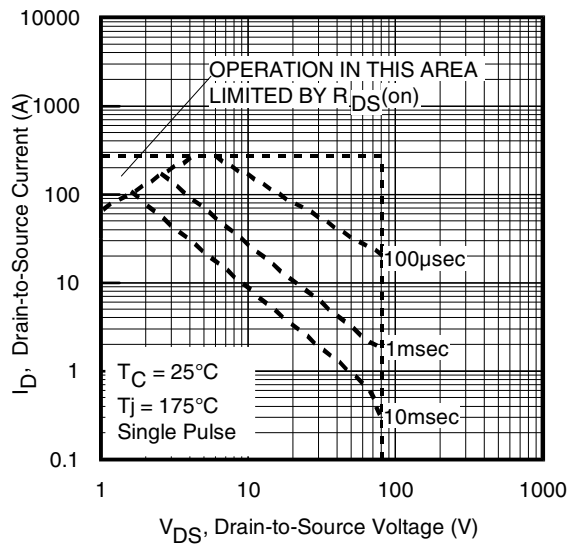
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area

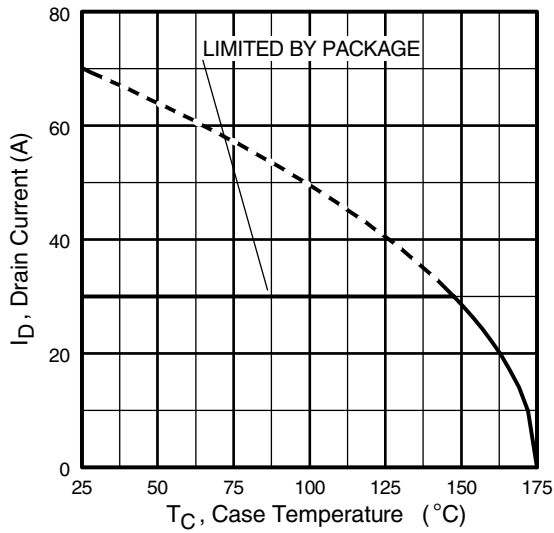


Fig 9. Maximum Drain Current Vs. Case Temperature

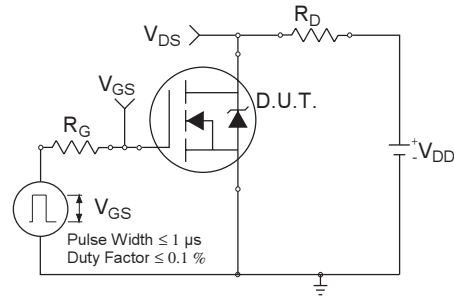


Fig 10a. Switching Time Test Circuit

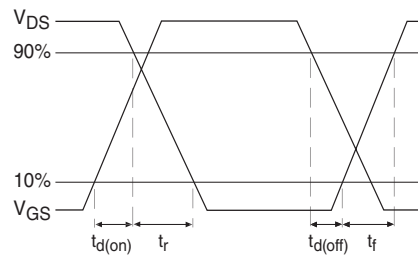


Fig 10b. Switching Time Waveforms

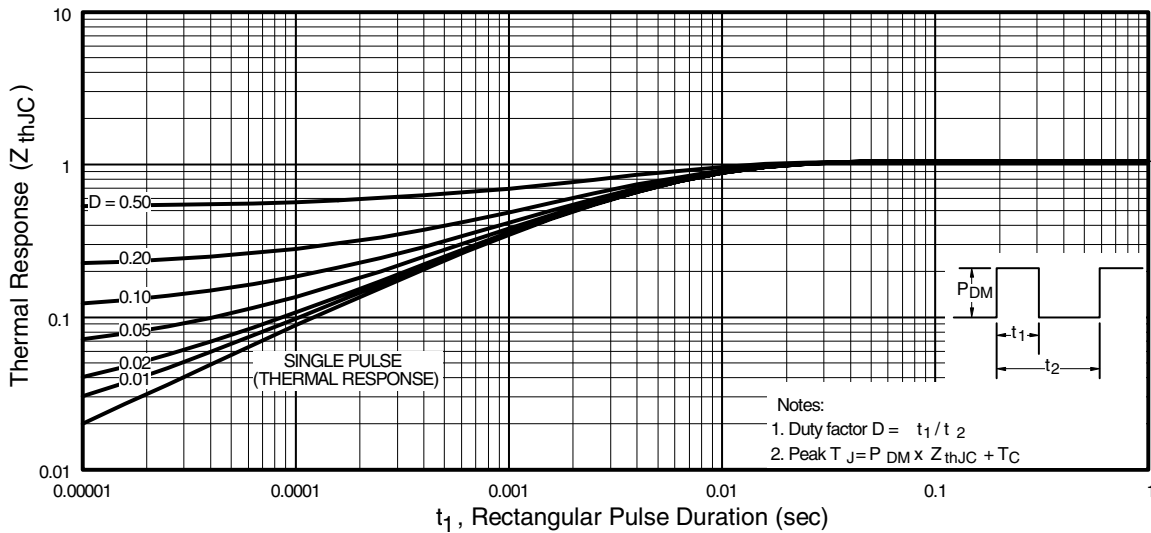
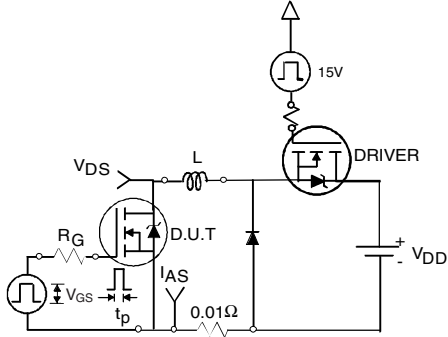
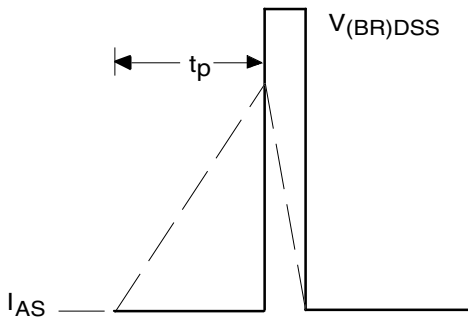


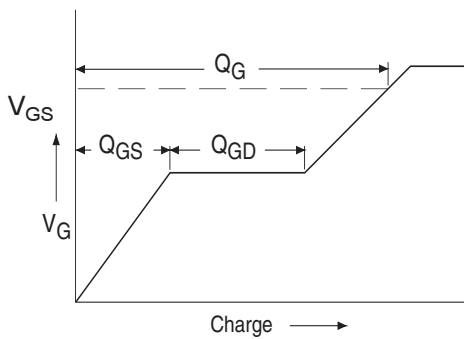
Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case



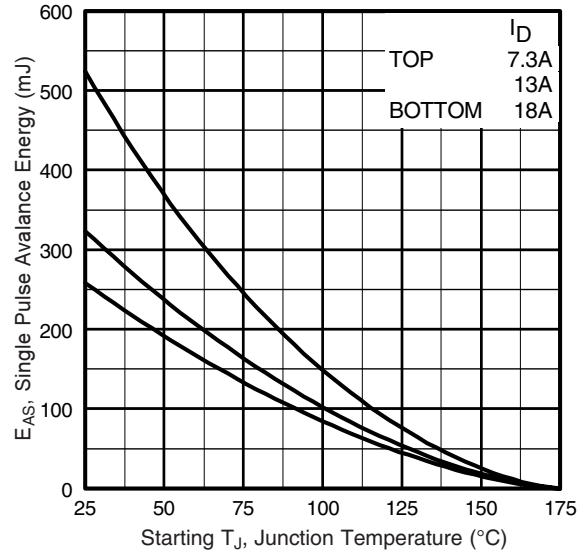
**Fig 12a.** Unclamped Inductive Test Circuit



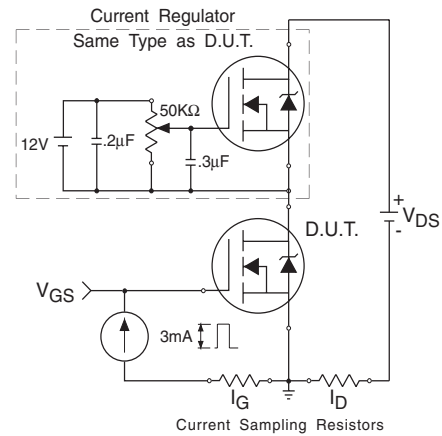
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform

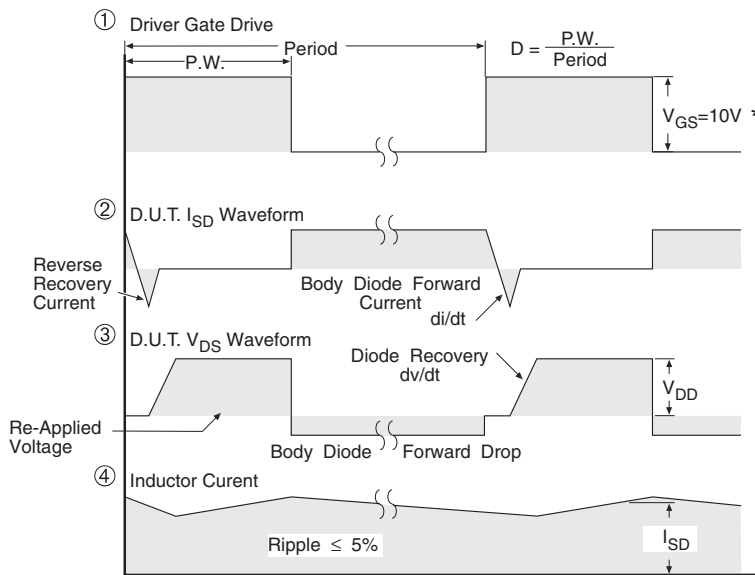
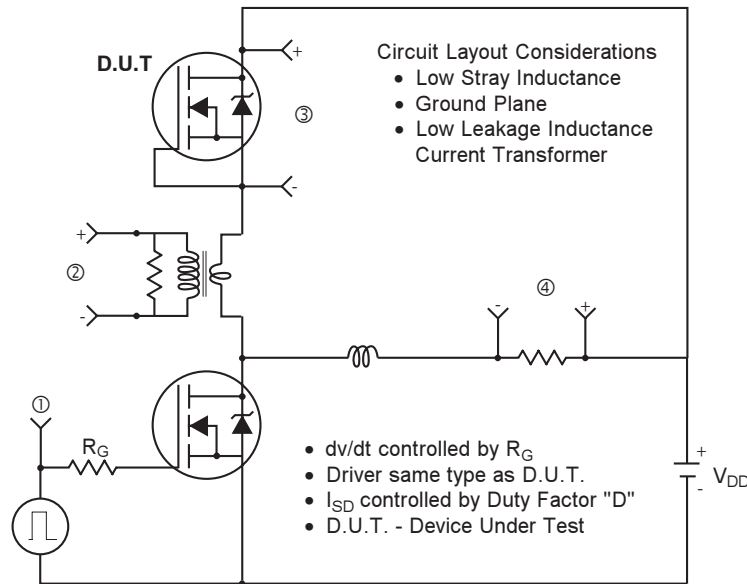


**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13b.** Gate Charge Test Circuit

**Peak Diode Recovery dv/dt Test Circuit**

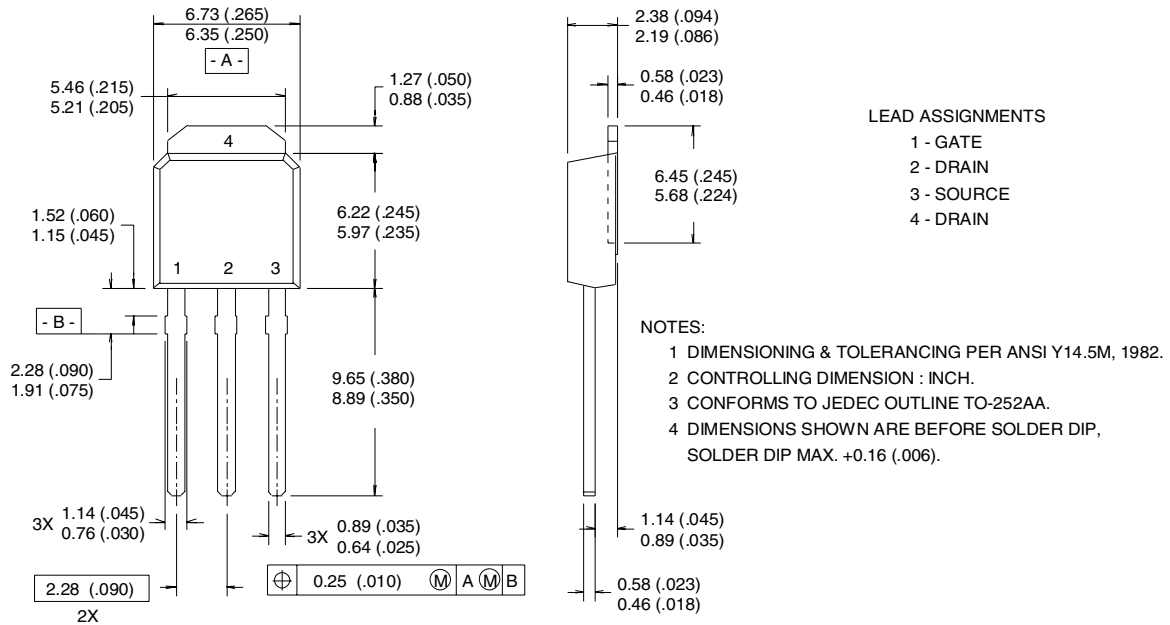


\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14.** For N-Channel HEXFET® Power MOSFETs

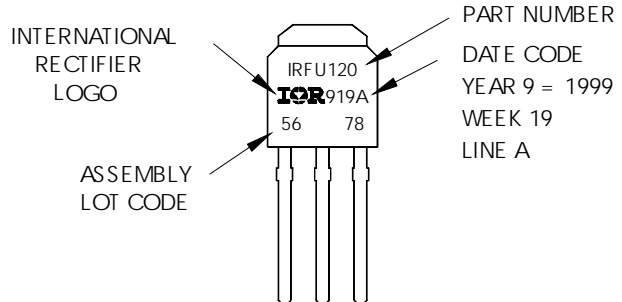
## TO-251AA (I-Pak) Package Outline

Dimensions are shown in millimeters (inches)



## TO-251AA (I-Pak) Part Marking Information

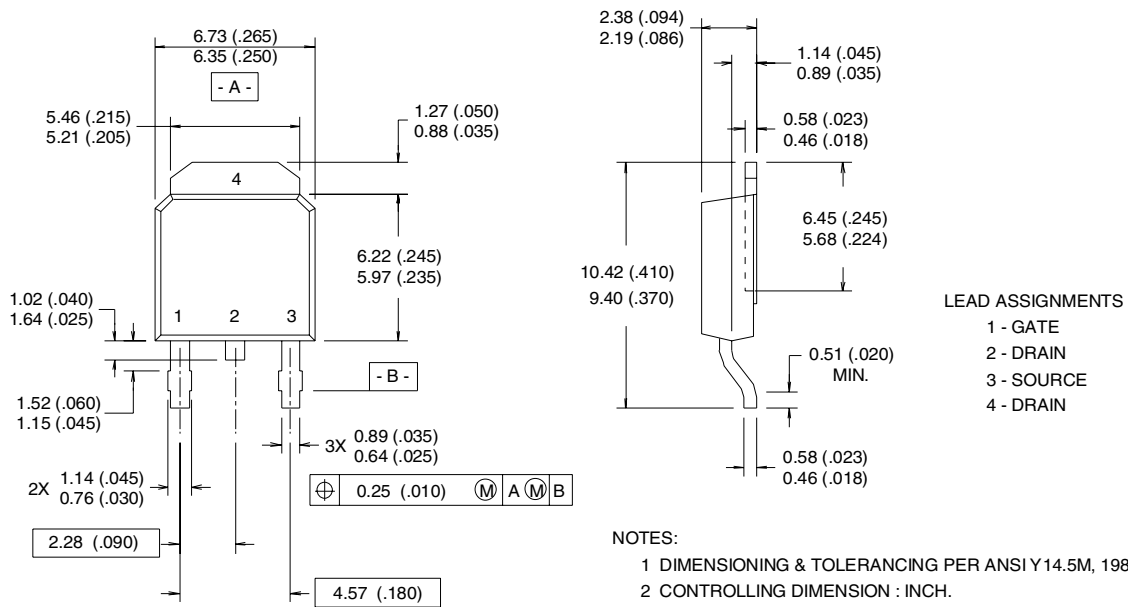
EXAMPLE: THIS IS AN IRFR120  
WITH ASSEMBLY  
LOT CODE 5678  
ASSEMBLED ON WW 19, 1999  
IN THE ASSEMBLY LINE "A"





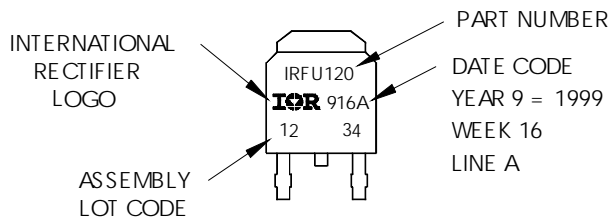
## TO-252AA (D-Pak) Package Outline

Dimensions are shown in millimeters (inches)



## TO-252AA (D-Pak) Part Marking Information

EXAMPLE: THIS IS AN IRFR120  
 WITH ASSEMBLY  
 LOT CODE 1234  
 ASSEMBLED ON WW 16, 1999  
 IN THE ASSEMBLY LINE "A"

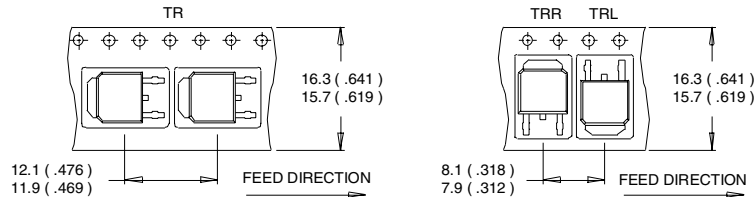


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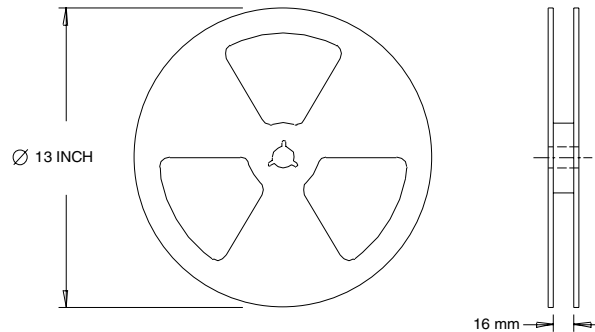
## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



**NOTES :**

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



**NOTES :**

1. OUTLINE CONFORMS TO EIA-481.

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 1.6\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 18\text{A}$ .
- ③  $I_{SD} \leq 18\text{A}$ ,  $di/dt \leq 350\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  
 $T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss}$  eff. is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 30A.

\* When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web site.

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