



# PSMN2R0-30YL

N-channel 30 V 2 m $\Omega$  logic level MOSFET in LPAK

Rev. 4 — 10 March 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in industrial and communications applications.

### 1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

### 1.3 Applications

- Class-D amplifiers
- DC-to-DC converters
- Motor control
- Server power supplies

### 1.4 Quick reference data

Table 1. Quick reference data

| Symbol                         | Parameter                        | Conditions   | Min | Typ  | Max | Unit             |
|--------------------------------|----------------------------------|--|-----|------|-----|------------------|
| $V_{DS}$                       | drain-source voltage             | $T_j \geq 25\text{ }^\circ\text{C}$ ; $T_j \leq 175\text{ }^\circ\text{C}$   | -   | -    | 30  | V                |
| $I_D$                          | drain current                    | $T_{mb} = 25\text{ }^\circ\text{C}$ ; $V_{GS} = 10\text{ V}$ ;<br>see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>                | [1] | -    | 100 | A                |
| $P_{tot}$                      | total power dissipation          | $T_{mb} = 25\text{ }^\circ\text{C}$ ; see <a href="#">Figure 2</a>   | -   | -    | 97  | W                |
| $T_j$                          | junction temperature             |  | -55 | -    | 175 | $^\circ\text{C}$ |
| <b>Static characteristics</b>  |                                  |  |     |      |     |                  |
| $R_{DS(on)}$                   | drain-source on-state resistance | $V_{GS} = 10\text{ V}$ ; $I_D = 15\text{ A}$ ;<br>$T_j = 25\text{ }^\circ\text{C}$   | -   | 1.55 | 2   | m $\Omega$       |
| <b>Dynamic characteristics</b> |                                  |  |     |      |     |                  |
| $Q_{GD}$                       | gate-drain charge                | $V_{GS} = 4.5\text{ V}$ ; $I_D = 10\text{ A}$ ;<br>$V_{DS} = 12\text{ V}$ ; see <a href="#">Figure 14</a> ;<br>see <a href="#">Figure 15</a> | -   | 7.5  | -   | nC               |



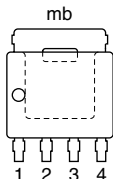
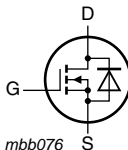
**Table 1. Quick reference data ...continued**

| Symbol                      | Parameter                                    | Conditions   | Min | Typ | Max | Unit |
|-----------------------------|--|--|-----|-----|-----|------|
| $Q_{G(\text{tot})}$         | total gate charge                            | $V_{GS} = 4.5 \text{ V}; I_D = 10 \text{ A};$<br>$V_{DS} = 12 \text{ V};$ see <a href="#">Figure 14</a>  | -   | 30  | -   | nC   |
| <b>Avalanche ruggedness</b> |  |  |     |     |     |      |
| $E_{DS(\text{AL})S}$        | non-repetitive drain-source avalanche energy | $V_{GS} = 10 \text{ V}; T_{j(\text{init})} = 25 \text{ }^\circ\text{C};$<br>$I_D = 100 \text{ A}; V_{\text{sup}} \leq 30 \text{ V};$<br>$R_{GS} = 50 \text{ } \Omega;$ unclamped | -   | -   | 151 | mJ   |

[1] Continuous current is limited by package.

## 2. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description                       | Simplified outline  | Graphic symbol   |
|-----|--------|-----------------------------------|---|--|
| 1   | S      | source                            |  <p style="text-align: center;">SOT669 (LPAK)</p> |  <p style="text-align: center;">mbb076</p> |
| 2   | S      | source                            |   |  |
| 3   | S      | source                            |   |  |
| 4   | G      | gate                              |   |  |
| mb  | D      | mounting base; connected to drain |   |  |

## 3. Ordering information

**Table 3. Ordering information**

| Type number  | Package |  |         |
|--------------|---------|--|---------|
|              | Name    | Description  | Version |
| PSMN2R0-30YL | LPAK    | plastic single-ended surface-mounted package (LPAK); 4 leads | SOT669  |

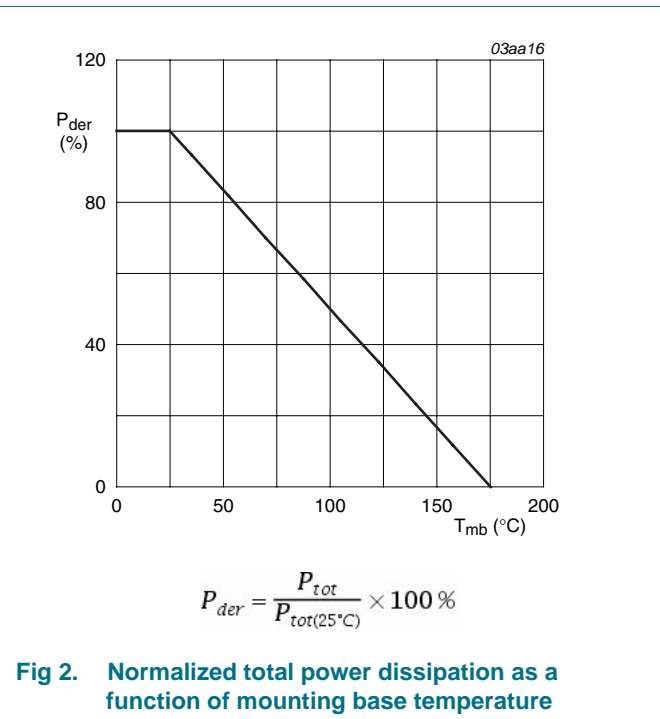
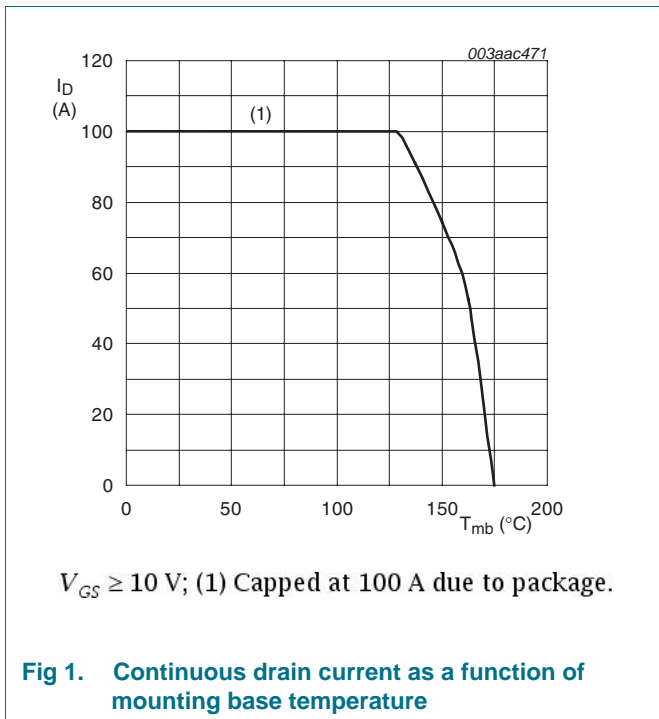
### 4. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol                      | Parameter                                    | Conditions   | Min | Max | Unit |
|-----------------------------|--|--|-----|-----|------|
| V <sub>DS</sub>             | drain-source voltage                         | T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C  | -   | 30  | V    |
| V <sub>DSM</sub>            | peak drain-source voltage                    | t <sub>p</sub> ≤ 25 ns; f ≤ 500 kHz;<br>E <sub>DS(AL)</sub> ≤ 280 nJ; pulsed   | -   | 35  | V    |
| V <sub>DGR</sub>            | drain-gate voltage                           | T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C; R <sub>GS</sub> = 20 kΩ   | -   | 30  | V    |
| V <sub>GS</sub>             | gate-source voltage                          |  | -20 | 20  | V    |
| I <sub>D</sub>              | drain current                                | V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; see <a href="#">Figure 1</a>   | [1] | 100 | A    |
|                             |  | V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; see <a href="#">Figure 1</a> ;<br>see <a href="#">Figure 3</a>                                | [1] | 100 | A    |
| I <sub>DM</sub>             | peak drain current                           | pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C;<br>see <a href="#">Figure 3</a>   | -   | 667 | A    |
| P <sub>tot</sub>            | total power dissipation                      | T <sub>mb</sub> = 25 °C; see <a href="#">Figure 2</a>  | -   | 97  | W    |
| T <sub>stg</sub>            | storage temperature                          |  | -55 | 175 | °C   |
| T <sub>j</sub>              | junction temperature                         |  | -55 | 175 | °C   |
| <b>Source-drain diode</b>   |  |  |     |     |      |
| I <sub>S</sub>              | source current                               | T <sub>mb</sub> = 25 °C  | [1] | 100 | A    |
| I <sub>SM</sub>             | peak source current                          | pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C  | -   | 667 | A    |
| <b>Avalanche ruggedness</b> |  |  |     |     |      |
| E <sub>DS(AL)S</sub>        | non-repetitive drain-source avalanche energy | V <sub>GS</sub> = 10 V; T <sub>j(initial)</sub> = 25 °C; I <sub>D</sub> = 100 A;<br>V <sub>sup</sub> ≤ 30 V; R <sub>GS</sub> = 50 Ω; unclamped | -   | 151 | mJ   |

[1] Continuous current is limited by package.



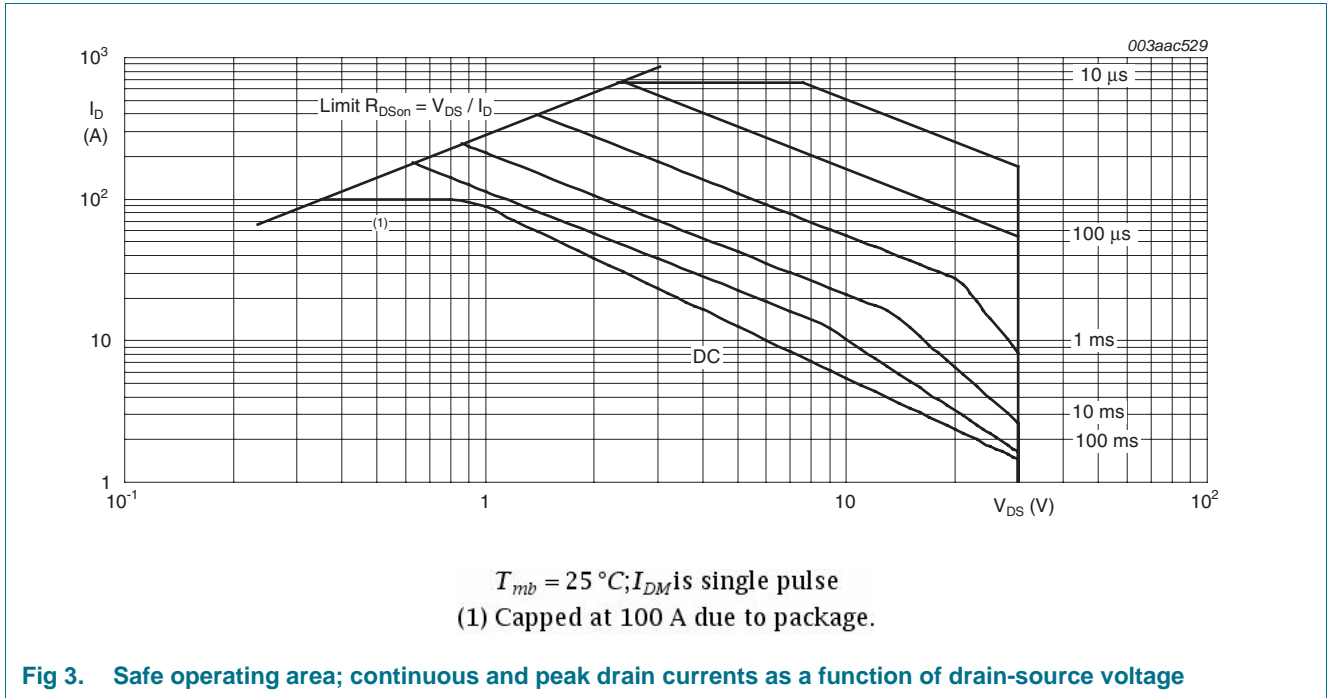


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

### 5. Thermal characteristics

Table 5. Thermal characteristics

| Symbol         | Parameter   | Conditions                   | Min | Typ | Max  | Unit |
|----------------|---|------------------------------|-----|-----|------|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | see <a href="#">Figure 4</a> | -   | 0.4 | 1.28 | K/W  |

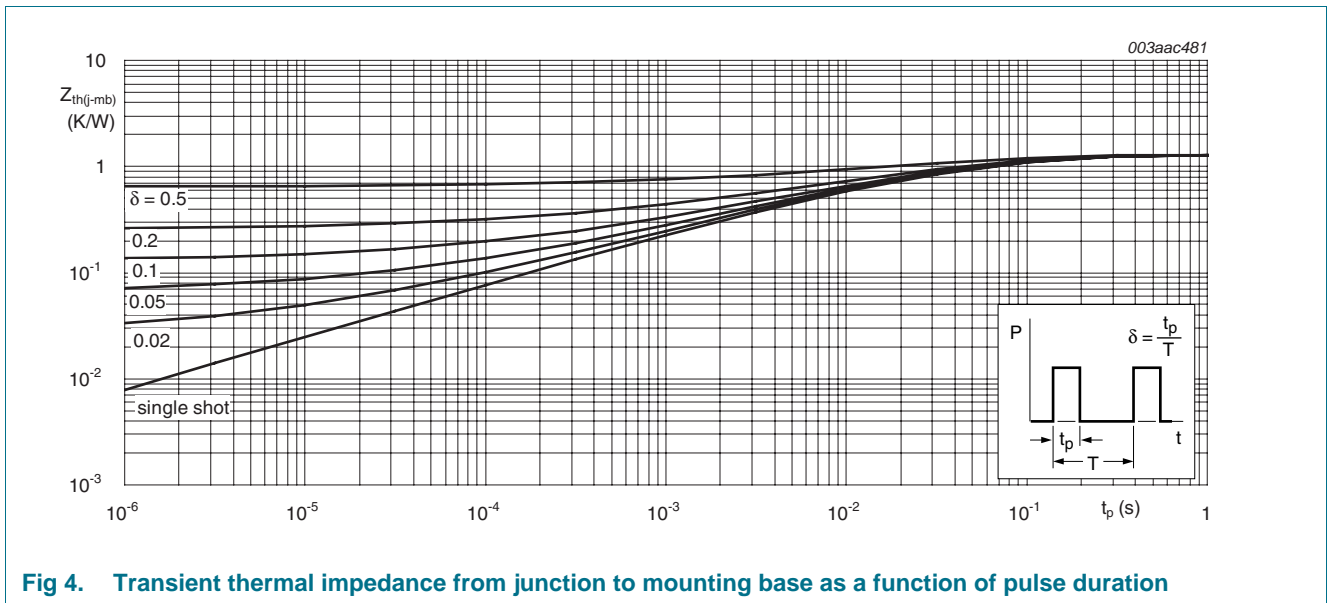


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 6. Characteristics

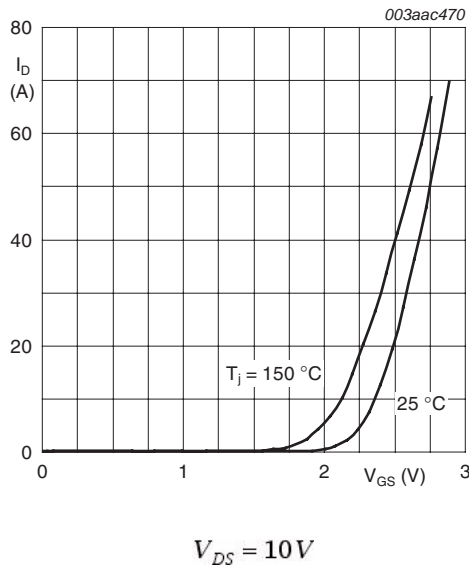
**Table 6. Characteristics**

Tested to JEDEC standards where applicable.

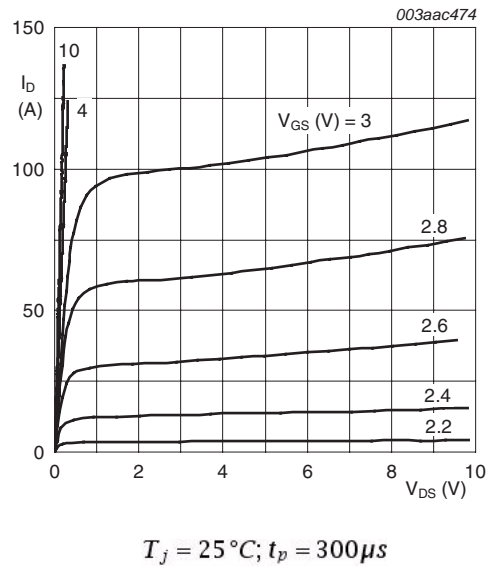
| Symbol                         | Parameter                         | Conditions   | Min  | Typ  | Max  | Unit    |
|--------------------------------|-----------------------------------|--|------|------|------|---------|
| <b>Static characteristics</b>  |                                   |  |      |      |      |         |
| $V_{(BR)DSS}$                  | drain-source breakdown voltage    | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$   | 30   | -    | -    | V       |
|                                |                                   | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$  | 27   | -    | -    | V       |
| $V_{GS(th)}$                   | gate-source threshold voltage     | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a> | 1.3  | 1.7  | 2.15 | V       |
|                                |                                   | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ C$ ; see <a href="#">Figure 12</a>                                | 0.65 | -    | -    | V       |
|                                |                                   | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$ ; see <a href="#">Figure 12</a>                                | -    | -    | 2.45 | V       |
| $I_{DSS}$                      | drain leakage current             | $V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$   | -    | -    | 1    | $\mu A$ |
|                                |                                   | $V_{DS} = 30 V; V_{GS} = 0 V; T_j = 150 \text{ }^\circ C$  | -    | -    | 100  | $\mu A$ |
| $I_{GSS}$                      | gate leakage current              | $V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$   | -    | -    | 100  | nA      |
|                                |                                   | $V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$  | -    | -    | 100  | nA      |
| $R_{DS(on)}$                   | drain-source on-state resistance  | $V_{GS} = 4.5 V; I_D = 15 A; T_j = 25 \text{ }^\circ C$  | -    | 2.13 | 2.63 | mΩ      |
|                                |                                   | $V_{GS} = 10 V; I_D = 15 A; T_j = 150 \text{ }^\circ C$ ; see <a href="#">Figure 13</a>  | -    | -    | 3.3  | mΩ      |
|                                |                                   | $V_{GS} = 10 V; I_D = 15 A; T_j = 25 \text{ }^\circ C$   | -    | 1.55 | 2    | mΩ      |
| $R_G$                          | gate resistance                   | $f = 1 \text{ MHz}$  | -    | 0.75 | 1.5  | Ω       |
| <b>Dynamic characteristics</b> |                                   |  |      |      |      |         |
| $Q_{G(tot)}$                   | total gate charge                 | $I_D = 10 A; V_{DS} = 12 V; V_{GS} = 10 V$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>                       | -    | 64   | -    | nC      |
|                                |                                   | $I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$   | -    | 59   | -    | nC      |
|                                |                                   | $I_D = 10 A; V_{DS} = 12 V; V_{GS} = 4.5 V$ ; see <a href="#">Figure 14</a>  | -    | 30   | -    | nC      |
| $Q_{GS}$                       | gate-source charge                | $I_D = 10 A; V_{DS} = 12 V; V_{GS} = 4.5 V$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>                      | -    | 9.8  | -    | nC      |
| $Q_{GS(th)}$                   | pre-threshold gate-source charge  |  | -    | 6.6  | -    | nC      |
| $Q_{GS(th-pl)}$                | post-threshold gate-source charge |  | -    | 3.2  | -    | nC      |
| $Q_{GD}$                       | gate-drain charge                 |  | -    | 7.5  | -    | nC      |
| $V_{GS(pl)}$                   | gate-source plateau voltage       | $V_{DS} = 12 V$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>  | -    | 2.34 | -    | V       |
| $C_{iss}$                      | input capacitance                 | $V_{DS} = 12 V; V_{GS} = 0 V; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 16</a>                      | -    | 3980 | -    | pF      |
| $C_{oss}$                      | output capacitance                |  | -    | 857  | -    | pF      |
| $C_{rss}$                      | reverse transfer capacitance      |  | -    | 347  | -    | pF      |
| $t_{d(on)}$                    | turn-on delay time                | $V_{DS} = 12 V; R_L = 0.5 \text{ } \Omega; V_{GS} = 4.5 V; R_{G(ext)} = 4.7 \text{ } \Omega$                                     | -    | 39   | -    | ns      |
| $t_r$                          | rise time                         |  | -    | 65   | -    | ns      |
| $t_{d(off)}$                   | turn-off delay time               |  | -    | 63   | -    | ns      |
| $t_f$                          | fall time                         |  | -    | 28   | -    | ns      |

**Table 6. Characteristics ...continued**  
Tested to JEDEC standards where applicable.

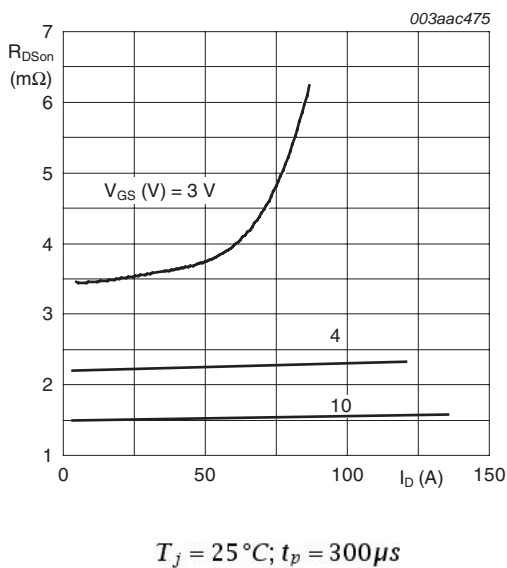
| Symbol                    | Parameter             | Conditions  | Min | Typ  | Max | Unit |
|---------------------------|-----------------------|---|-----|------|-----|------|
| <b>Source-drain diode</b> |                       |   |     |      |     |      |
| $V_{SD}$                  | source-drain voltage  | $I_S = 25\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$ ;<br>see <a href="#">Figure 17</a> | -   | 0.78 | 1.2 | V    |
| $t_{rr}$                  | reverse recovery time | $I_S = 20\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ;                 | -   | 43   | -   | ns   |
| $Q_r$                     | recovered charge      | $V_{DS} = 20\text{ V}$  | -   | 49   | -   | nC   |



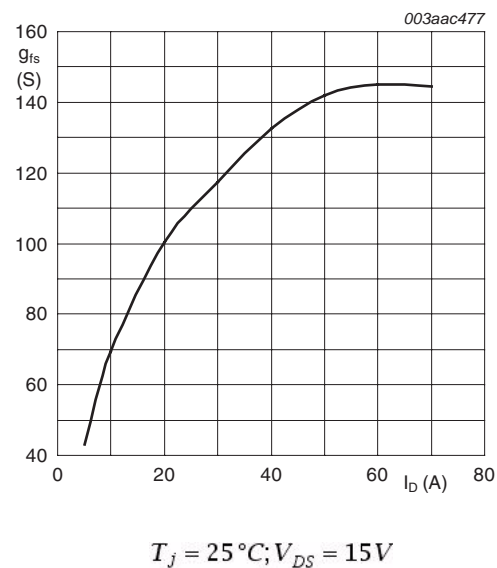
**Fig 5. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



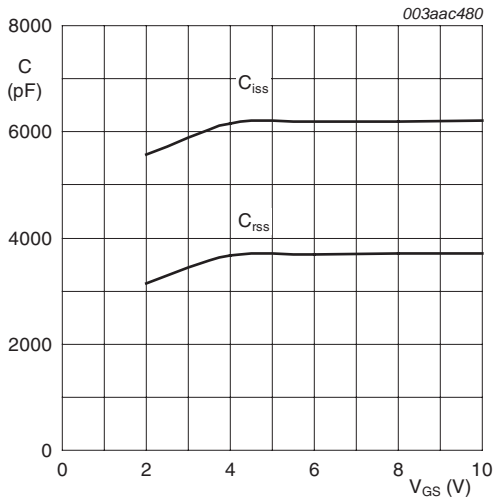
**Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values**



**Fig 7. Drain-source on-state resistance as a function of drain current; typical values**

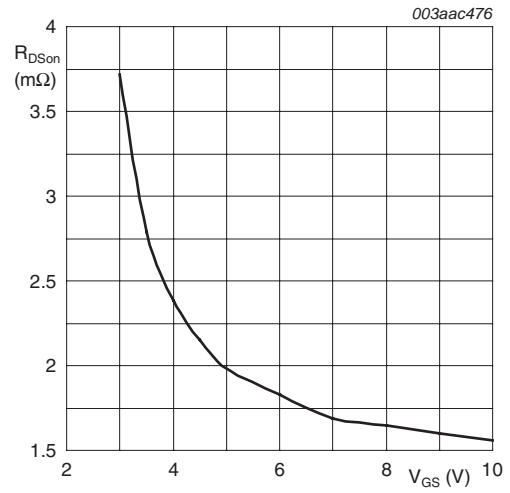


**Fig 8. Forward transconductance as a function of drain current; typical values**



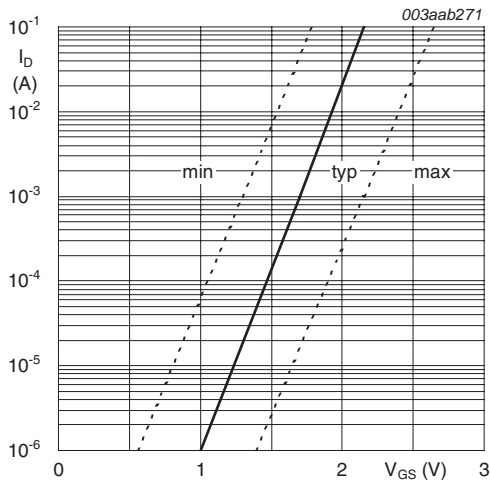
$V_{DS} = 0V; f = 1MHz$

Fig 9. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



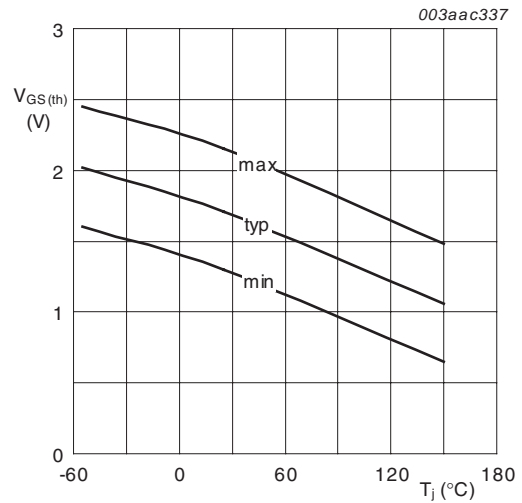
$T_j = 25^\circ C; I_D = 15A$

Fig 10. Drain-source on-state resistance as a function of gate-source voltage; typical values



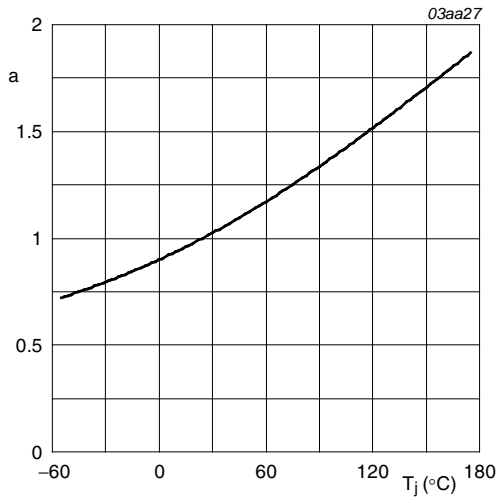
$T_j = 25^\circ C; V_{DS} = 5V$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



$I_D = 1mA; V_{DS} = V_{GS}$

Fig 12. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

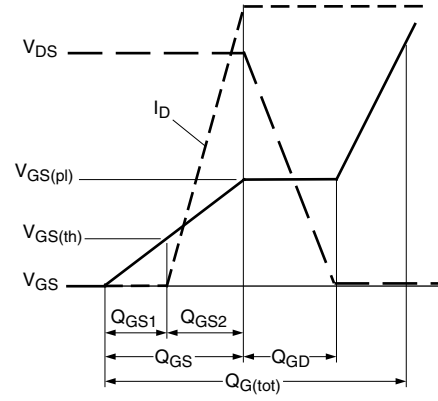
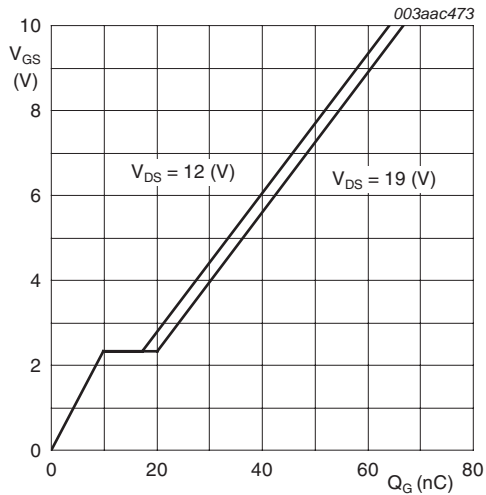
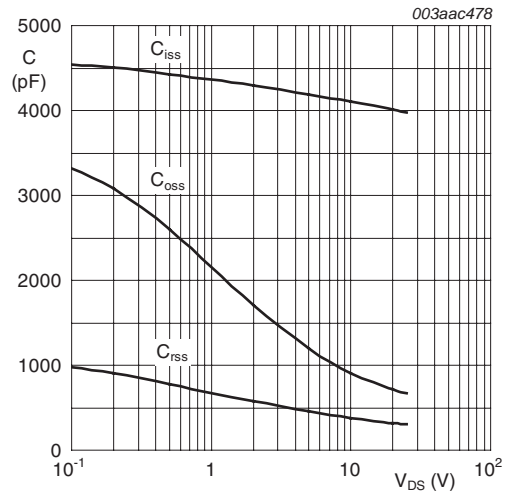


Fig 14. Gate charge waveform definitions



$$T_j = 25^{\circ}C; I_D = 10A$$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$$V_{GS} = 0V; f = 1MHz$$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



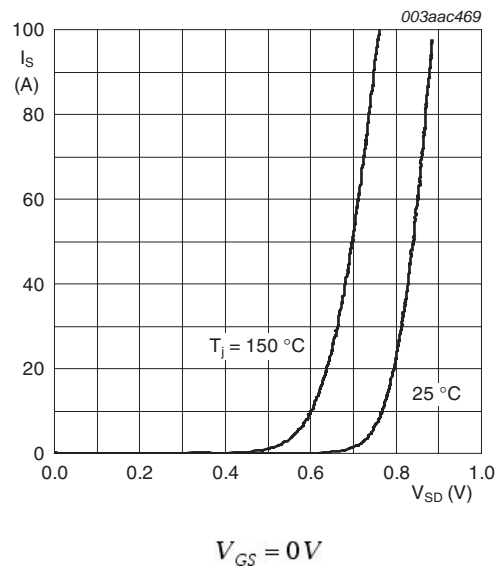


Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LPAK); 4 leads

SOT669

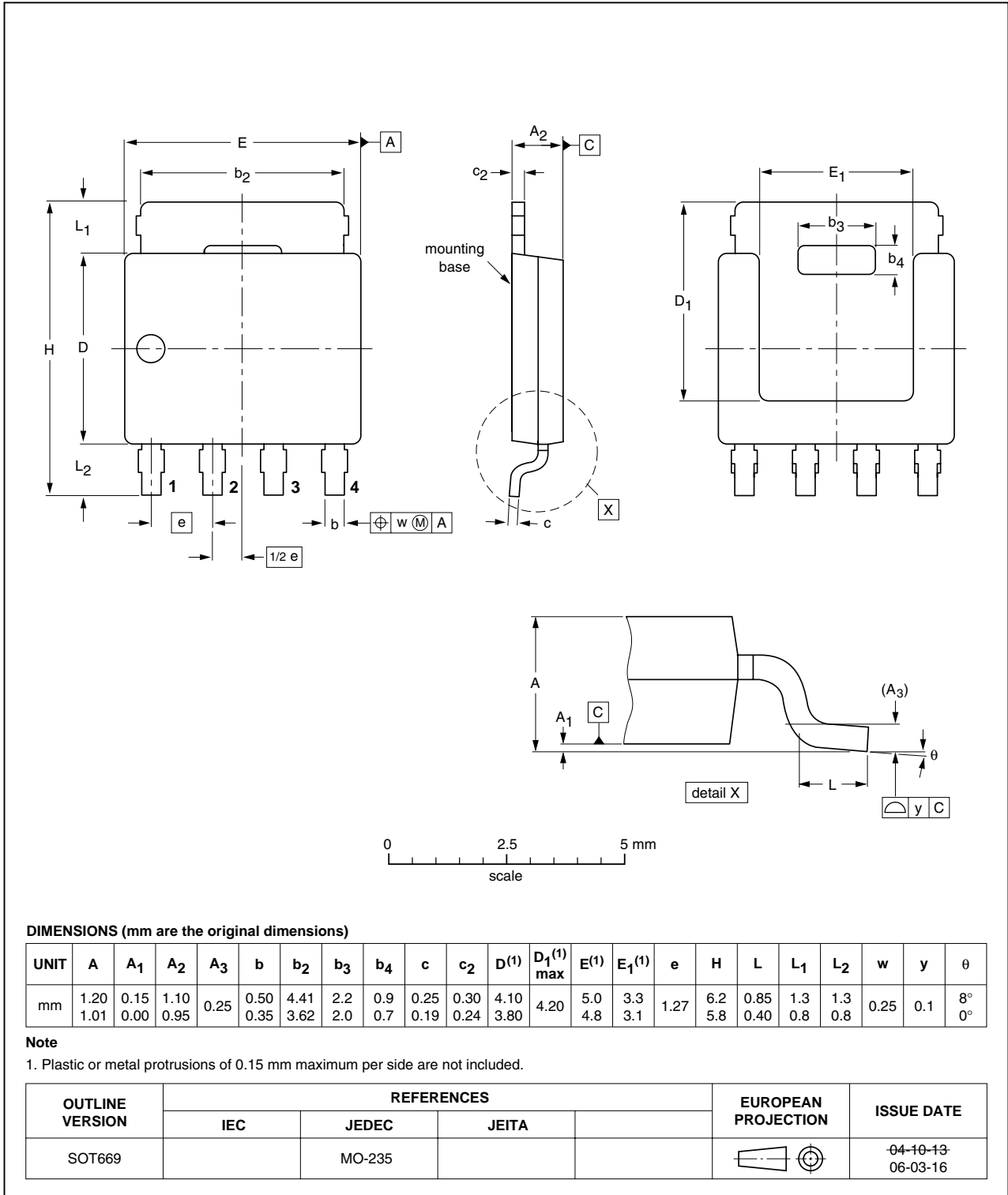


Fig 18. Package outline SOT669 (LPAK)

## 8. Revision history

Table 7. Revision history

| Document ID      | Release date                  | Data sheet status  | Change notice | Supersedes     |
|------------------|-------------------------------|--------------------|---------------|----------------|
| PSMN2R0-30YL v.4 | 20110310                      | Product data sheet | -             | PSMN2R0-30YL_3 |
| Modifications:   | • Various changes to content. |                    |               |                |
| PSMN2R0-30YL_3   | 20090105                      | Product data sheet | -             | PSMN2R0-30YL_2 |

## 9. Legal information

### 9.1 Data sheet status

| Document status <sup>[1]</sup> <sup>[2]</sup> | Product status <sup>[3]</sup> | Definition  |
|---|-------------------------------|---|
| Objective [short] data sheet                  | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet                | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet                    | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 11. Contents

|           |  |           |
|-----------|--|-----------|
| <b>1</b>  | <b>Product profile</b> . . . . .         | <b>1</b>  |
| 1.1       | General description . . . . .            | 1         |
| 1.2       | Features and benefits . . . . .          | 1         |
| 1.3       | Applications . . . . .                   | 1         |
| 1.4       | Quick reference data . . . . .           | 1         |
| <b>2</b>  | <b>Pinning information</b> . . . . .     | <b>2</b>  |
| <b>3</b>  | <b>Ordering information</b> . . . . .    | <b>2</b>  |
| <b>4</b>  | <b>Limiting values</b> . . . . .         | <b>3</b>  |
| <b>5</b>  | <b>Thermal characteristics</b> . . . . . | <b>4</b>  |
| <b>6</b>  | <b>Characteristics</b> . . . . .         | <b>5</b>  |
| <b>7</b>  | <b>Package outline</b> . . . . .         | <b>10</b> |
| <b>8</b>  | <b>Revision history</b> . . . . .        | <b>11</b> |
| <b>9</b>  | <b>Legal information</b> . . . . .       | <b>12</b> |
| 9.1       | Data sheet status . . . . .              | 12        |
| 9.2       | Definitions . . . . .                    | 12        |
| 9.3       | Disclaimers . . . . .                    | 12        |
| 9.4       | Trademarks . . . . .                     | 13        |
| <b>10</b> | <b>Contact information</b> . . . . .     | <b>13</b> |

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